Buildup and Characterization of an Active Flexible Microelectrode Array

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Alles Sprechen und Schreiben heißt Würfeln um den Gedanken.
Wie oft fällt nur ein Auge, wenn alle sechs fallen sollten.

Friedrich Hebbel

Summary

The integration of CMOS-dies into flexible electrically active implants offers numerous new opportunities for smart implants. Due to a closed control loop such implants can measure and analyze body signals, before reacting to them with a specific response. This work was conducted as part of a project aiming for the development of a new kind of microelectrode array based on an array of small dies. Therefor a complete fabrication process starting with the separation and assembly of the dies, continuing with their embedding into a foil, and ending with the fabrication of conducting tracks connecting the dies was developed.
For the transfer and embedding of the dies a selective transfer printing process based on a silicone stamp was developed. The transfer of a subgroup of dies allows the increase of the spacing of neighboring dies to any integer multiple. The process works reliable with a yield between 90% and 100%. The maximum strength the stamps can pull off dies from a tape was determined. For a stamp with a profile of $(300\,\mu\mathrm{m})^2$ square bumps it is – depending on the softness of the PDMS – $65\,$kPa or $83\,$kPa for a peeling speed of $10\,\frac{\mathrm{mm}}{\mathrm{min}}$.
To equalize the height of the dies they were embedded in silicone. The die array was placed upside down in a thin shellac film before it was cast in silicone. Spacers together with a covering glass guaranteed for a homogeneous layer thickness. After curing of the silicone the shellac was used as a release layer. The resulting surface topography has an amplitude $< 10\,\mu\mathrm{m}$.
This surface then allows the structuring of conducting tracks and VIAs (vertical interconnect access) using processes based on photolithography. To fabricate conducting tracks Ti/Au/Ti was sputter deposited on the surface and then dry etched against a resist mask. Etching of the VIAs required the structuring of an aluminum hardmask, as the surface moved in the vacuum leading to the formation of cracks in a resist mask.
The different process steps have been successfully combined to build a demonstrator system based on inoperable die-dummies. For the demonstrator system a 7×7 array of die-dummies with a size of $250\,\mu\mathrm{m} \times 250\,\mu\mathrm{m} \times 200\,\mu\mathrm{m}$ each was embedded and electrically connected by two layers of conducting tracks. The system could be completely built, but failure during fabrication lead to both interrupted and short-circuited tracks. Thus, no electrical measurements were possible with the system.
The location of the neutral axis within the system can be calculated using a simple model. Its location within the layer system can be set by proper variation of the thickness of the different material layers.
For any application of an electrically active implant inside the body the longtime stability of the device is of outstanding importance. Flexible systems cannot use rigid hermetic housings.
Atomic layer deposition (ALD) is a method allowing the deposition of defect free layers of

high quality. Within this work Al_2O_3 and TiO_2 films have been successfully deposited at temperatures $< 120°C$ using ALD. Measurements of ALD coated foils showed up to 18,571 times lower helium leak rates than uncoated foils. This is a distinct sign for the excellent barrier properties of the ALD layers.

Zusammenfassung

Die Integration von CMOS-Chips in flexible elektrisch aktive Implantate eröffnet zahlreiche neue Möglichkeiten für intelligente Implantate, die in einem geschlossenen Regelkreis Körperwerte ermitteln und verarbeiten, um dann gezielt darauf zu reagieren. Diese Arbeit wurde im Zuge eines Projekts zur Entwicklung eines neuartigen Mikroelektrodenarrays auf Basis eines Arrays kleiner ungehäuster Chips erstellt. Dazu wurde ein vollständiger Herstellungsprozess ausgehend von der Vereinzelung und der Anordnung der Chips, über deren Einbettung in eine Folie, bis hin zur Herstellung der die Chips verbindenden Leiterbahnen entwickelt.
Zum Übertragen und Anordnen der Chips wurde ein selektiver Transfer Printing Prozess mit einem Silikonstempel entwickelt. Durch das Übertragen einer Subgruppe von Chips kann der Abstand benachbarter Chips auf ein ganzzahliges Vielfaches vergrößert werden. Der Prozess funktioniert zuverlässig mit einer Übertragungsquote zwischen 90% und 100%. Die maximalen Kräfte, mit denen die Silikonstempel Chips von einer Klebefolie abziehen können wurden ermittelt und betragen für Stempel mit einem Profil aus $(300\,\mu m)^2$ großen Erhebungen je nach Härte des Silikons $65\,$kPa bzw. $83\,$kPa bei einer Abzugsgeschwindigkeit von $10\,\frac{mm}{min}$.
Um die Höhe der Chips auszugleichen wurden die Chips in Silikon eingebettet. Dazu wurde das Chip-Array mit den Chipoberseiten nach unten in eine dünne Schellackschicht gesetzt und mit Silikon übergossen. Abstandshalter am Rand im Zusammenspiel mit einem Deckglas sorgten für eine homogene Schichtdicke. Nach dem Aushärten des Silikons diente die Schellackschicht als Trennschicht. Die Topographie der aus dem Einbettungsprozess resultierenden Oberfläche hatte eine Amplitude $< 10\,\mu m$.
Diese Oberfläche ermöglichte die Strukturierung von Leiterbahnen und Durchkontaktierungen mittels photolithographischer Prozesse. Für die Leiterbahnen wurde Ti/Au/Ti aufgesputtert und gegen eine Lackmaske trocken geätzt. Um Durchkontaktierungen durch das Parylen ätzen zu können musste eine Aluminiumhartmaske strukturiert werden, da sich die Oberfläche im Vakuum bewegte, was in einer Lackmaske zur Rissbildung führte.
Die einzelnen Prozessschritte wurden erfolgreich zusammengefügt, um ein auf funktionslosen Chip-Dummys basierendes Demonstratorsystem aufzubauen. Für das Demonstratorsystem wurde ein Array aus 7×7 Chip-Dummys mit einer Größe von jeweils $250\,\mu m \times 250\,\mu m \times 200\,\mu m$ eingebettet und mit zwei Leiterbahnebenen verbunden. Das System ließ sich komplett aufbauen, aber Fehler während der Herstellung führten sowohl zu unterbrochenen als auch zu kurzgeschlossenen Leiterbahnen. Daher waren keine elektrischen Messungen mit dem System möglich.
Die Lage der neutralen Ebene innerhalb des Systems kann mit einem einfachen Model berechnet werden. Ihre Lage im Schichtsystem lässt sich durch die Variation der Schichtdicke

einzelner Lagen gezielt einstellen.
Für Anwendungen im Körper ist die Langzeitstabilität elektrisch aktiver Implantate von herausragender Bedeutung. Flexible Systeme können dabei nicht auf ein starres hermetisches Gehäuse zurückgreifen.
Atomlagenabscheidung (ALD) ist ein Verfahren, das die Abscheidung defektfreier Schichten hoher Güte erlaubt. Im Zuge dieser Arbeit wurden erfolgreich Al_2O_3 und TiO_2 Schichten mittels ALD bei niedrigen Temperaturen $\leq$ 120°C abgeschieden. Messungen an mittels ALD beschichteten Folien wiesen eine um bis zu 18.571-fach reduzierte Heliumleckrate gegenüber unbeschichteten Folien auf. Dies ist ein deutlicher Hinweis auf die hervorragenden Barriereeigenschaften der ALD-Schichten.

Abbreviations

ALD	atomic layer deposition
BIF	barrier improvement factor
CMOS	complementary metal-oxide-semiconductor
CVD	chemical vapor deposition
GPC	growth per cycle
MEA	microelectrode array
MEMS	microelectronic and microelectromechanical systems
PDMS	polydimethylsiloxane (group of silicones)
PEALD	plasma-enhanced atomic layer deposition
PECVD	plasma-enhanced chemical vapor deposition
PVD	physical vapor deposition
RIE	reactive ion etching
SEM	scanning electron microscope
TMA	trimethylaluminium (precursor for the deposition of Al_2O_3)
TTIP	titanium tetraisopropoxide (precursor for the deposition of TiO_2)
VIA	vertical interconnect access
WVTR	water vapor transmission rate

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Chapter 1

Motivation and Objectives

Motivation

Microelectrode Arrays (MEAs) are valuable tools widely used for electrophysiological measurements. Microelectrode arrays can be classified into *active* and *passive* MEAs. While active MEAs are highly integrated chips with integrated electrical circuits, passive MEAs are simple devices connecting each electrode with a contact on the periphery of the device. However, as each electrode is connected to a conducting track the possible electrode density or the number of electrodes of one array is limited, respectively.
This work was conducted within the project "NEURO-FLEXARRAY"[1] aiming for a new kind of microelectrode array. The Neuroflexarray (NFA) is intended to be a hybrid combining the advantages of *active* and *passive* MEAs by integrating an array of micro-dies into a flexible foil.
The dies were developed within the project and fulfill two tasks. Multiplexing reduces the number of required conducting tracks, which allows an increase of the number of electrodes of one array. Signal amplification close to the electrodes increases the signal-to-noise ratio.
The Neuroflexarray as a flexible MEA is also intended for *in vitro* applications and thus has to struggle with the same demands as smart implants. Different smart implants have already shown their high potential in modern medicine, e.g. by measuring body signals and reacting due to a feed-back loop with a controlled stimulation. They can cure or at least bring relief for diseases such as: cardiac arrhythmia [1, 2], epilepsy [3], Parkinson's [4, 5] and loss of bladder control [6]. In some cases they can even restore lost senses, at least when the nerves are not damaged. For a loss of hearing cochlear implants are in use [7], while retina implants can to some degree restore sight [8, 9].
In the long term there will be more and more new systems for use in different parts of the body, correcting malfunctions in the body or restoring lost functions. New therapy approaches with these "electroceuticals" will replace conventional pharmaceuticals and have the advantage that they have less side effects [10].
The intelligence of these implants is based on electronic circuitry within the implant, which then

[1] sponsored by the Federal Ministry of Education and Research, Germany (grant 13FH031IA5)

has to be protected from the harsh humid body environment. Most electrically active implants so far possess a rigid housing for the protection of their delicate components. However, the mismatch between rigid housings and soft body tissue is a disadvantage that cannot always be accepted. Thus, flexible smart implants have to be developed.
The longtime stability of electrically active implants in the wet body environment is a central issue. As the flexibility of a smart implant is incompatible with rigid hermetic housings made of titanium, glass or ceramics new solutions have to be developed. The main source of failure is water entering the implant. Most sensitive are of course all electrically active components.
Thin metal oxide layers with low defect densities can be used as barrier layers, preventing or at least significantly decreasing the intrusion of water into a foil implant. Atomic layer deposition (ALD) is a highly sophisticated chemical vapor deposition method providing layers of high conformity and extremely low defect densities that are hence suitable as barrier layers. To decrease temperature during deposition plasma enhanced ALD processes can be used allowing temperatures of $120°C$ or less being compatible with polymeric materials of flexible implants.

Research Objectives

The aim of this work was to develop a fabrication process for the device envisioned within the project "NEURO-FLEXARRAY". This fabrication process had to include a process for the assembly of dies with an edge length of only $250\,\mu m$ and a process for the embedding of an array of these dies into a flexible polymer foil providing a surface allowing the use of thin-film fabrication techniques on top. Further, processes to structure conducting tracks and VIAs (vertical interconnect access) on top of the embedded dies had to be developed. In addition Al_2O_3 and TiO_2 films were deposited using plasma enhanced ALD and characterized to exploit their possible use as water vapor barrier layers, increasing the longtime stability of polymer based flexible implants.

Chapter 2

Introduction

2.1 smart implants

There are different categories of implants, ranging from cosmetic implants (e.g. breast implants) and functional implants (e.g. RFID-Chip underneath the skin) to medical implants. Medical implants can be passive, as stents stabilizing blood vessels and hip prostheses, or active e.g. pacemakers. This work is focused on electrically active implants. Active implants that exhibit a certain "intelligence" making them "smart" are sometimes called smart implants. Such implants not only actively influence the body, but also actively modify their function to changing situations. As the "intelligence" of a smart implant might have its source in electronic circuitry smart implants can also be electrically active implants, although the two terms in general are not synonymous. This section is about smart electrically active implants. It starts by giving a short introduction on the significance of electrical signals in the human body, then shows the potential of influencing these signals for medical applications and ends giving concrete examples for smart implants in the aforementioned sense that have lead to the term "electroceutical" [10].

2.1.1 electrical signals in the human body

At the end of the eighteenth century the role of electricity in the body was discovered. Luigi Galvani experimented with different metals and animal muscles and observed the contraction of frog legs connected to two different metals being in contact with each other. However, it was Alessandro Volta drawing the right conclusion that the frogs leg was an indicator and not the source of the electricity originating from the contact of the two different metals (contact potential difference or *volta potential*). In the nineteenth century Carlo measured currents from pigeon heart muscle. Also the field of electrophysiology was established by Johannes Müller, Emil du Bois-Reymond and Hermann von Helmholtz. They discovered that neurons use electrical excitations to communicate.

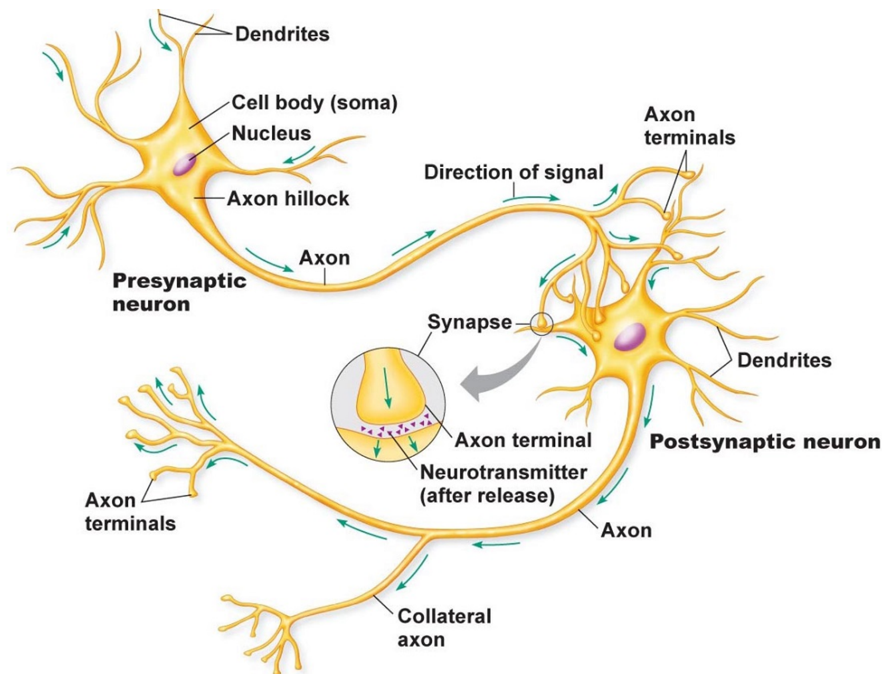


Figure 2.1: Sketch of two neurons, showing their cell body, the dendrites and the axon with the axon terminals at their end. The two neurons are connected over the synapse between the axon terminals of the first neuron and the dendrites of the second neuron. (taken from `https://www.printablediagram.com` (July 16, 2019))

the neuron

The neuron (nerve cell) consists of different parts: the soma, the dendrites, the axon and the axon terminals (Fig. 2.1) [11]. The soma is the cell body responsible for the metabolism. The dendrites are the parts receiving electrical excitations from other neurons. The axon or nerve fiber carries the electrical excitation. The axon terminals are part of the synapse which is the contact structure of two neurons. Between the inside and the outside of the cell – defined by the cell membrane – there is a potential difference of about - 80 mV. This potential is called resting membrane potential. It originates from different concentrations of ions in the electrolyte. For example the concentration of potassium ions is higher in the inside, while the concentration of sodium ions is higher outside the cell. The ion concentrations are determined by different permeability of the membrane for the different ions, diffusion and ion-currents due to electrical voltages. The Na^+/K^+ pump is responsible for the concentration of the sodium and potassium ions. It pumps them against their concentration gradients.

the action potential

When the membrane potential of the cell is increased above the threshold of about - 50 mV the permeability of the membrane for the sodium ions increases and the potential rises up to about + 40 mV. This is called depolarisation. As the slower potassium channels also open the potential decreases again and the membrane repolarizes. After the threshold is exceeded a

well-defined process is started, independent of further stimuli. It is therefore also called an *all or nothing* process. Thus, all neural information is binary coded. After the triggering of the action potential, the cell membrane is completely insensitive for a certain time. The threshold is increased and decreases with time before reaching the value of the resting state. This refractory period takes around 2 ms and limits the signal rate at which a neuron can transmit [11].
The action potential does not occur in the complete neuron at once, but travels along the axon – that can be up to > 1 m long – and hence transmits the electrical excitation. When a section of the axon is depolarized and ions flow through the membrane this leads to a changed electrical field. This causes instantaneously a force on ions in neighboring sections of the axon, where as a result the electrical voltage between the inside and the outside of the membrane changes, leading to the depolarization in this neighboring section. Thus the excitation travels along the axon towards the synapse.

the synapse

The synapse is the structure allowing for the transfer of information from one neuron to another. The main parts of this structure are the presynaptic terminal, the synaptic cleft and the postsynaptic terminal. When an action potential reaches the presynaptic terminal it leads to a release of neurotransmitters. These chemical messengers diffuse through the synaptic cleft and bind to receptor molecules at the postsynaptic terminal which leads to a change of the postsynaptic potential. The sum of the potential changes due to different neurotransmitters reaching the post-synaptic neuron – distributed on several synpases – can then cause this neuron to become active and start an action potential [11].

2.1.2 therapy through the control of electrical signals

After identifying electrical signals as information flow within the body it is obvious that their recording can give insight in the functioning or malfunctioning of the body. Recording the electrical signals means listening to the body on a fundamental level and thus their control could allow the therapy of malfunctionings – causing a disease – on a fundamental level. While some psychopharmaceuticals work on the conduction of these signals by blocking or influencing their transmittance in the synapse – where the signal is transmitted chemically via a neurotransmitter – they cannot be applied spatially restricted and then come with significant side effects.
Targeted electrical manipulation of the body is a possible alternative to treat chronic diseases. While it is difficult to control the region and duration of effect of pharmaceuticals once they are launched into the body, electrical stimulation can – depending on the electrodes – be performed in a spatially and temporally controlled way, without affecting other parts of the body.
Therapy using electrical stimulation is not aimed on looking on symptoms – that are a body response due to a disease – or on infections that are caused by an external attack from bacteria or viruses. It aims on malfunctions of the body itself. Thousands of control and regulation loops regulate all aspects of living. Receptors measure for example the CO_2 partial pressure in the blood to trigger breathing. In another control loop of the body other receptors measure the blood glucose concentration which is then controlled via the release of insulin. Diabetes

describes the case where this control loop does not work properly. Any malfunctioning of such a control loop in the body is a possible target for electrical stimulation and smart implants [12]. Closing or replacing such a loop however is not only done by stimulation, but requires also the determination of the right moment and intensity. So a medical device for such a task has to be a closed-loop system too, requiring sensors and a circuitry for the interpretation of their data enabling it to respond appropriately, which could in the easiest case be stimulation or no stimulation. As such devices, healing on a bioelectronic level, could in some cases replace common pharmaceuticals the term “electroceutical” [10] has been suggested.

Such devices have three potential sites where they can interface to the nervous system [13]. The first place is the organ itself, which can for example be a muscle. The second possibility is interfacing the peripheral nervous system and the third is to interface the central nervous system. Direct interfacing of the brain and the central nervous system appears to be a tempting possibility, because as the central control unit of the body it in principle offers boundless possibilities. However, interfacing to the brain or central nervous system requires excellent knowledge on where different body functions are controlled. Stimulation at the wrong position can cause fatal side effects. The peripheral nervous system offers easier specific access. Still, the sensitive tissue makes both, interfacing the central and peripheral nervous system, a challenging task. So it is very attractive to directly interface the end organ. However, different kind of electrodes have been developed to interface nerves [13].

Nerves are bundles of many nerve fibers. Cuff electrodes are wrapped around the nerve and are in clinical use for example for vagus nerve stimulation [14, 15]. FINE (flat interface nerve electrode) electrodes also enclose the nerve but in contrast to the normal cuff electrodes compress and reshape the nerve leading to smaller distance of the inner nerve fibers to the surface [16].

Other more invasive electrodes directly contacting the targeted fiber, leading to higher sensitivity and selectivity, have been developed and tested in several studies, e.g. LIFE (longitudinal intrafascicular electrode) and TIME (transverse intrafascicular electrode) electrodes [17].

The Michigan array [18] and the Utah array [19] are two famous examples for silicon based penetrating electrode arrays fabricated with MEMS fabrication technology. For the Michigan array shafts are structured from silicon that have several electrodes on their side. Several of these shafts can be combined to a comb like structure and several of these combs can build up an three dimensional array with up to 1024 electrodes [18, 20]. The Utah array is an array of 100 needles with an electrode at their tip. Each needle is separated from its neighbors by $400\,\mu\mathrm{m}$ [19].

2.1.3 application of smart implants

There are several smart implants currently in clinical use, some of them for decades. However, their technology has been adapted to more and more new fields of use, and progress in fabrication technology together with better understanding of the body will allow the fabrication of better and new kinds of smart implants addressing different organs and diseases.

Figure 2.2: Left: Sketch showing how the cochlear implant is placed in the ear. Right: Picture of the implanted part of the system with the electrode shaft in front. (pictures taken from `www.medel.com/ch/image-gallery` (July 30, 2019))

cardiac pacemaker

The cardiac pacemaker is somehow the grandfather of many of the currently used smart implants, concerning its technology. As electrocardiography (ECG) is the most prominent example for electricity in the body it is not surprising, that devices were built to trigger heart beat in patients. The first cardiac pacemaker was implanted in 1958 with a lifetime of few hours, directly followed by the second with a lifetime of several days [1]. Since then the device has tremendously improved. One topic has always been power supply. The first cardiac pacemaker implanted in Germany had a life-time of only 18 months. So to solve the power supply problem in the 70s nuclear batteries were used. Also concepts to recharge the device from outside have been developed and used. Today modern batteries lead to lifetimes of 5 to 12 years [2]. Another topic has been the stability of electronics in the body. While the first implanted pacemakers were rather primitive devices housed in epoxy resin. Today's pacemakers define the standard for a many different smart implants with their batteries and electronics packed in a hermetic metal housing. For the connection of the electrode with cables the housing has feed-throughs. While the electrode has to be at the heart the pacemaker itself can be placed at a more easily accessible place. Also, while the first pacemakers have been simple pulse generators modern pacemakers are rather smart devices, as they adapt their stimulation frequency due to stress related parameters e.g. due to physical activity of the patient [21].

cochlear implant

Cochlear implants (see Fig. 2.2) are also a very successful example for a smart implant already used for several decades with more than 100,000 deaf persons having received cochlear implants [7,22]. While the outer ear only collects the sound and helps to locate the direction of the sounds origin, the middle ear makes an impedance matching between the sound traveling in air in the outer ear and the fluid filled system of the inner ear. In the inner ear the pressure wave is then

converted to an electrical signal carrying the information to the brain.
In the inner ear the sound waves travel along the basilar membrane separating two fluid filled tubes running along the coil of the cochlea. Due to change of its mechanical stiffness and geometry different frequencies show maxima at different positions along the basilar membrane leading to a spatial encoding of different sound frequencies and thus enabling the differentiation of different tone pitchs [23]. Hair cells then perform the actual conversation to electrical signals. The cochlear implant can replace this part of the hearing system when the hair cells are lost. A microphone outside the body collects the sound and a speech processor generates a stimulation pattern that is then transferred to the implanted part of the cochlea implant. A silicone based electrode shaft with up to 22 electrodes implanted into the cochlea then directly stimulates the acoustic nerve at different positions using different electrodes along the electrode shaft to represent different frequencies within the sound [7, 22, 23].
The implant itself looks quite similar to a cardiac pacemaker using the same kind of hermetic metal or ceramics housing to protect its electronics.

retina implant

Another smart implant restoring a lost sense, at least to a certain degree, is the retina implant. Similar to the case of the cochlea implant information is again encoded in the position of an electrical stimulation. In the case where only the photoreceptor cells transducing the light into electrical signals are lost retina implants can replace their function and electrically stimulate the retina due to a perceived image [8, 9, 24]. There are different possibilities for the realization of such a device, including three possible locations where to place the electrode array [9]. With a subretinal implant including photodiodes as well as stimulation electrodes on one single chip only the lost function of the photoreceptor cells is replaced, while the optical system of the eye as well as signal processing of the eye is further used [24].
Due to the anatomical conditions the retina implant needs to be very small and flexible and therefore can not use the approved design of implants as the cardiac pacemaker or the cochlear implant.

Flexible smart implants are a promising cure or at least therapy for many diseases. An example, where the feasibility of curing a malfunction of the body with a smart implant has been shown, is diabetes [25, 26]. The technological realization requires new concepts and is thus still part of current research [27, 28].

2.2 MEA-technology

While the last section introduced some electrode forms for different applications in smart implants this section is about arrays of microelectrodes, this means a flat field of many regular arranged electrodes. Of course such an array can potentially be transformed in a electrode as mentioned in the section above. For example a flat array can be rolled up to enclose a nerve.
A microelectrode array (MEA) – sometimes multielectrode array – is a device with multiple pads or pins through which neural signals can be obtained or delivered and therefore make

another observable accessible. They build electrical interfaces between tissue and electronic circuitry. While in the measuring instrument all currents are due to electron flow, in the body the electrical signal transmission is due to ion flow. So the main task of the electrode contacting the body tissue is the conversion of the ionic conduction in the electrolyte of the body into electronic conduction in the measurement electronics.
For different applications a lot of different MEAs are used, some for *in vitro* others for *in vivo* applications. MEAs not only allow the recording of the cells on the electrodes but also their electrical stimulation [29].
In vitro cells can be cultivated in a very controlled environment on the MEA while their electrical activity is recorded. Transparent MEAs allow for simultaneous observation under the microscope. This makes MEAs a proper tool to examine the cells reaction on different disturbances [30–32]. MEAs have established as a tool in pharmacological studies [33, 34] or to unravel the behavior of neural networks [35].
In vivo MEAs can provide insight in neurological process related to diseases. Implanted electrode grids on the brain for example are an important tool in epilepsy treatment. They can help to localize epileptogenic areas that can be removed prior to surgery [36].
In future MEAs could build human-machine interfaces that can be used to control prostheses [37].

2.2.1 electrophysiology

intracellular recording

For intracellular recording an electrode is inserted into the cell. With an electrode inside the cell it is possible to measure the voltage or current flow to a reference electrode outside the cell. However, damaging the cell-membrane of course limits the life-time of the cell. Different procedures for intracellular recordings have been developed. A glass micropipette filled with electrolyte offers good access to the inner of the cell as electrode.
In the voltage clamp technique two electrodes are inserted into the cell. A transmembrane voltage is set between the inner of the cell and an outside reference electrode. A current electrode then passes current into the cell to hold this "command potential". This current is opposite to the ionic current through the cell membrane.
In the current clamp technique the membrane potential is free to vary and the amplifier records the potential set by the cell itself.
For the patch clamp technique a micropipette with an opening diameter of about $1\,\mu\mathrm{m}$ is brought near the cell and a slight underpressure is applied. A reference electrode is placed in the extracellular fluid surrounding the cell. Several different variants are possible to measure either only a few or even only one ion channel or the complete cell. Patch clamp can be performed using the voltage clamp or the current clamp technique. To measure only individual ion channels cell-attached, inside-out and outside-out method can be used. For cell-attached procedure underpressure is applied, until a region of the cell membrane is suctioned into the micropipette forming a seal with an electrical resistance of $10 - 100\,\mathrm{G\Omega}$. The cell membrane stays intact so there is only little disturbance for the cell. This allows the measurement of

currents through the ion channels included in the region enclosed by the micropipette. The inside-out and outside-out methods are disruptive, ending with only a little patch of the cell membrane connected to the micropipette. The inside-out method starts as the cell-attached method with the pipette attached to the cell membrane but then removes the pipette from the rest of the cell tearing off the patch connected to the cell with the seal. While the outside of the membrane is then connected to the inside of the pipette the intracellular surface is exposed to the bath. The outside-out method proceeds from another starting point, ending with the patch being the other way round so that the intracellular surface of the membrane is attached to the micropipette and the extracellular surface is exposed to the bath. To measure the complete cell the whole-cell method can be used. Therefor, cell-attached configuration is used as a starting point, but then the membrane is disrupted within the micropipette so that the inside of the cell is connected to the inside of the micropipette.

extracellular recording

Extracellular recording is noninvasive to the cell, as it does not require perforation of the cell membrane. Thus, the cells' lifetimes are not shortened, making extracellular recording suitable for *in vitro* but also for *in vivo* experiments. The ion currents flowing through the cell membranes and the change in voltage between the inside and the outside of the cells cause voltage changes in the environment of the cell. The electrodes in extracellular recording record these changes in reference to a more distant reference electrode and convert the ion flow caused by the cells into an electron flow for the measurement system (Fig. 2.3) [38, 39]. As the signals detected by extracellular recording are about three orders of magnitude smaller in their amplitude as signals detected by intracellular recording, only the spikes of action potentials can be detected [40]. The signal amplitude and frequency range strongly depends on the cell type and distance from the cell. The summed up potential from several nearby cells is called local field potential. Typical values for signals as reported are [41]:

- neuronal local field potentials: < 5 mV amplitude, 1 Hz - 300 Hz
- neuronal action potentials : < 1 mV amplitude, 300 Hz - 6 kHz
- cardiac action potentials : < 50 mV amplitude, 1 Hz - 1 kHz

The electrode can either be a passive metal electrode or a field-effect transistor acting as an amplifier [38, 40].

stimulation

Applying voltage or current pulses to microelectrodes can cause voltage gradients polarizing the membrane of cells attached to them leading to excitation or inhibition of electrical activity of those cells. There are then two mechanisms of charge transfer on the electrode/electrolyte interface. In non-faradaic processes no electrons are exchanged between electrode and electrolyte and the interface can be modeled as a capacitor where charges redistribute but do not cross the interface [29, 42]. Faradaic reactions include the transfer of electrons across the

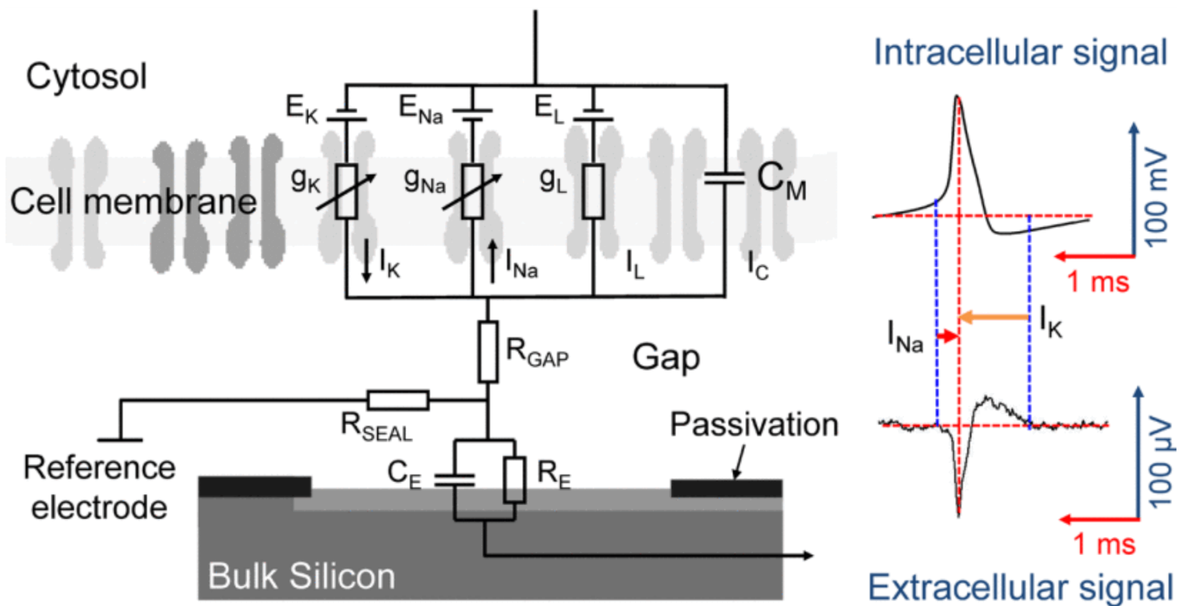
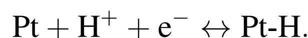


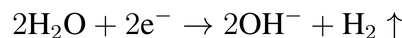
Figure 2.3: Electrical equivalent circuit of a cell membrane on a metal electrode. On the right side an intracellular neuronal signal from a patch clamp measurement is displayed besides a signal from extracellular recording showing the difference in signal amplitudes. Picture taken from [40] (©2011, IEEE).

electrode/electrolyte interface and are thus associated with chemical reactions [29, 42].
To avoid damage of the electrode or the tissue the stimulation pulses should include an anodal and a cathodal phase with an overall total charge flow of zero [29, 42]. Any net charge flow would move the electrode potential away from equilibrium and at some point induce irreversible reactions leading to corrosion of the electrode and possibly damage to the tissue [29, 42].
The reactions taking place on the electrode surface can either be reversible or irreversible. A reversible reaction would for example be the adsorption of hydrogen on a platinum electrode



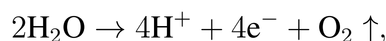
$$\mathrm{Pt} + \mathrm{H}^+ + \mathrm{e}^- \leftrightarrow \mathrm{Pt\text{-}H}.$$

Another reversible reaction would be monolayer oxidation formation and reduction. These processes affect only areas on the interface and do not produce new chemical species in the bulk of the solution [42]. Irreversible processes would for example be the reduction of water at a negative potential



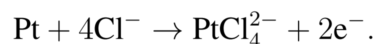
$$2\mathrm{H_2O} + 2\mathrm{e}^- \rightarrow 2\mathrm{OH}^- + \mathrm{H_2}\uparrow$$

and the oxidation of water at a positive potential



$$2\mathrm{H_2O} \rightarrow 4\mathrm{H}^+ + 4\mathrm{e}^- + \mathrm{O_2}\uparrow,$$

or the corrosion of platinum in chloride containing electrolyte:



$$\mathrm{Pt} + 4\mathrm{Cl}^- \rightarrow \mathrm{PtCl_4^{2-}} + 2\mathrm{e}^-.$$

Such irreversible reactions may introduce new, possibly toxic, products or alter the electrode and are therefore undesirable [42].

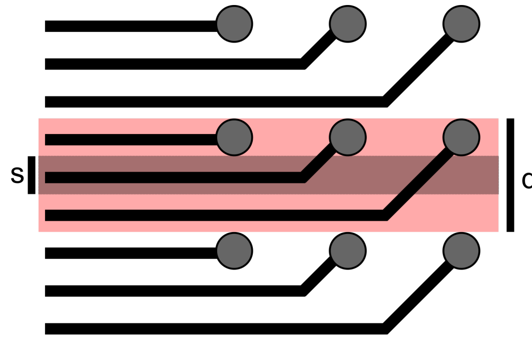


Figure 2.4: Schematic illustrating the situation in a passive MEA, where each electrode requires a separate conducing track. For an electrode spacing d and a spacing s for the tracks, there can only be d/s tracks per row and thus the number of electrodes is limited.

The amount of charge that can be safely injected depends on the electrode material, electrode size and real surface area that can be larger than the geometrical size of the electrode due to surface roughness. Different materials have shown to feature higher charge injection capacities and are thus better than simple metal electrodes, for example TiN [43] or carbon nanotubes [44].

2.2.2 state of the art MEAs

MEAs can be categorized into passive MEAs that are rather simple devices, and active MEAs that include active circuits and can be arbitrarily complex devices.

passive MEAs

For a passive microelectrode array each electrode is connected to a separate contact via a separate conducting track. The array only guides the electrical signals to the contact sites where it is connected to the measurement electronics. So it forms a completely passive device and there is no signal processing inside the array. As each electrode comes with its own track the electrode number and density are correlated and limited due to the finite space available to guide all the tracks. With each conducing track requiring the lateral extent s including the width of the track as well as the spacing to the next track for a given electrode spacing d there can only be d/s tracks in a row, which means there can only be d/s columns of electrodes (Fig. 2.4). When the contacts are allowed to be on all sides of the array, this array can of course be mirrored, guiding the same amount of tracks to the right side as to the left side.
However, it is clear that for a passive MEA from a certain point the number of electrodes can only be further increased without decreasing the electrode density by adding additional layers with conducting tracks or by going to new fabrication processes allowing for smaller track sizes s. Both solutions come with additional effort and decreasing signal quality. Additional layers come with longer tracks and VIAs (vertical interconnect access) increasing the electrical resistance between electrode and measurement unit. Also all these tracks are guided parallel and are thus capacitively coupled. Also smaller track sizes s increase the electrical resistance of the tracks. The input impedance of the measurement unit is extremely high leading to almost no

Table 2.1: A selection of different passive MEAs distributed from Multi Channel Systems MCS GmbH (Reutlingen, Germany).

name	# electrodes	electrode density (1/mm^2)	covered area (mm^2)	flexible
FlexMEA36	32	≈ 11	2.25	Yes
FlexMEA72	64	≈ 2	26.25	Yes
256MEA30	252	≈ 1111	0.20	No
256MEA60	252	≈ 278	0.81	No
256MEA100	252	100	2.25	No
256MEA200	252	25	9	No

current flow and thus the impedance of the tracks does not lower signal amplitude, but remains a source of noise. Thermal noise depends on the temperature and the ohmic resistance. Long tracks are also sensitive to disturbing signals from the environment causing artifacts.
Available MEAs normally have up to 252 electrodes and electrode densities between 2 and 1000 electrodes/mm^2 originating from electrode spacings between 30 μm and 1 mm. Table 2.1 refers to a selection of passive MEAs on the market giving their electrode number, electrode density and the area covered by electrodes. The big advantage of passive MEAs is that they can be fabricated on all kind of substrates, being rigid, flexible or stretchable.

active MEAs

Active microelectrode arrays place amplifiers as close as possible to the cells resulting in lower noise signals. Integrated circuits then also allow the addition of further features besides signal amplification and filtering aiming for lower noise and thus better signals. For example cyclic voltammetry, temperature sensors or light emitting diodes could bee added on the chip. Multiplexing can enable extremely high electrode densities and electrode numbers. Table 2.2 refers to a selection of active MEAs published in the last years. While they have up to 30,000 electrodes, their number of channels that can be measured in parallel often is lower. CMOS based MEAs can either follow an active-pixel sensor (APS) architecture, or an switch-matrix approach (SM). Due to the limited space MEAs following an active-pixel approach have to balance between spatial resolution, noise and power consumption. In addition their full-frame rate typically is less than 10 kHz. MEAs following an switch-matrix approach have less channels that can be read out in parallel, but as they are less constrained in area they allow the implementation of amplifiers with less noise [41]. CMOS MEAs cover only areas of few square millimeters and are non-flexible.
The electrode array presented by Viventi et al. [49] is none of the highly integrated CMOS-chips with extremely high electrode densities, but is a flexible active array. Each electrode is connected to the gate of a transistor working as amplifier. The drain of this transistor is then connected to a second transistor working as multiplexer. The different rows of the array can then be read out one after the other [50].

For the Neuroflexarray an array of tiny dies integrated into the array provides multiplexing,

Table 2.2: An overview on different active MEAs developed so far. Most of them are non-flexible CMOS-MEAs. The number of electrodes in the second column refers to the number of recording electrodes.

name	# electrodes	electrode density (1/mm^2)	covered area (mm^2)	flexible
CMOS-MEA16 [45,46]	4,225	$\approx$ 3906	1.05	No
CMOS-MEA32 [45,46]	4,225	$\approx$ 977	4.19	No
Eversmann et al. [47]	32,768	$\approx$ 12,987	2.60	No
Ballini et al. [41]	26,400	$\approx$ 3,265	8.10	No
Berdondini et al. [48]	4,096	$\approx$ 567	7.13	No
Viventi et al. [49]	360	4	90	Yes

reducing the number of required tracks and thus allowing for arrays with more electrodes than in a passive MEA. The dies also amplify the signals, making them more resistant against noise adding to the signals on the tracks transmitting them to the measurement unit. A low-pass filtering prevents aliasing during multiplexing, high-pass filtering is necessary to skip any DC offset and allow signal amplification.

2.2.3 development of new MEAs

Current developments aim for improvement in three major topics for current MEAs. First of all the mechanical properties of the array, so basically the fabrication of stretchable MEAs for *in vivo* as well as for *in vitro*. Second the electrode itself, including 3D electrodes providing better contact to the cells. Third there is research on active MEAs aiming on flexible active devices. Thinking of a planar device, flexible means that the device can be bend around one axis like a sheet of paper. This allows the device to better follow any shape given e.g. by an organ. Movement in the body however often comes along with the elongation and compression of surfaces that can not be matched with a flexible device. Thus, stretchable devices made of soft material that can easily be deformed (elongated and compressed) are required.
For *in vivo* applications it is obvious that rigid arrays are not suitable and that the mechanical properties of the device should match to those of the soft tissue [51]. There is a variety of materials suitable as base material for such an array as parylene C and polyimide as flexible materials, and PDMS as a stretchable material [52]. However, from the technological side the realization of the corresponding conducting tracks is difficult, as normal metal tracks are not stretchable. So there have been different efforts for such microelectrode arrays based on conductive polymer [53] or carbon nano-tubes [54]. The deposition of gold on prestretched substrates also resulted in stretchable conducting tracks [55]. As a static environment is unnatural, stretchable MEAs are also an issue for *in vitro* applications [56].
While for the electrodes there are materials providing good stability and charge transfer capacities, there is search for transparent electrodes with similar properties allowing the observation of the cells attached to the MEA from the backside. While indium tin oxide (ITO) can be used for transparent conducting tracks it shows poor electrochemical stability in contact with aqueous media. Therefore carbon nanotubes, graphene and conductive polymers have been used to fabricate transparent electrodes [57–59]. Another field of research are 3D electrodes

allowing better contact to the cells and thus better signals [39]. Martina et al. developed a batch fabrication process for three-dimensional MEAs, resulting in silicon cones with the electrodes on the tips of these cones [60]. Furthermore the desire for flexible active MEAs allowing higher electrode numbers and the integration of additional functions has already led to many different arrays. Pajouhi et al. developed a flexible microelectrode array based on CMOS islands of only $19\,\mu m \times 19\,\mu m$ size and a thickness of $10\,\mu m$ containing temperature sensors [61]. Winkin et al. developed a flexible microelectrode array by embedding CMOS dies into a polyimide foil. The dies are $2.64\,mm \times 2.02\,mm$ in size and only $20\,\mu m$ thick and are each connected to 25 stimulation electrodes [62]. Ohta et al. also developed a flexible MEA using an array of CMOS dies. They embedded up to 64 dies in epoxy resulting in an array with 576 electrodes, as each of their dies supports 9 electrodes [63, 64]. Pothof et al. developed a deep brain recording probe with 8 integrated CMOS dies amplifying, filtering and multiplexing each the signal of 16 recording electrodes [65]. The $40\,\mu m$ thick dies are first bonded to a planar polyimide foil, before the foil is then rolled up.

2.3 stability of microimplants

This section is on the fabrication of flexible electrically active implants that are fabricated using microfabrication processes. Although the term microimplant can imply several different implant classes including non-active implants, in the following the term only refers to smart implants as discussed in section 2.1 that are in addition flexible and fabricated using microfabrication processes. Such implants are not yet established but under development. As established CMOS fabrication technology allows cost efficient and high-quality fabrication of integrated circuits, the integration of unhoused chips – bare dies – into flexible polymer foils is a promising route towards flexible smart systems providing many possibilities. The fabrication of such a chip-in-foil system though is a challenging task and different processes have been proposed.
In this section therefore different processes for the fabrication of chip-in-foil systems and microimplants are discussed. The advantages and disadvantages of the different fabrication paradigms are discussed, before a review of concrete processes that have been published in the literature is given. Afterwards the repertory of materials that is used for the fabrication of flexible implants is presented. Finally failure mechanisms of microimplants in the above mentioned meaning are briefly discussed, before presenting routes for increasing their longtime stability. The last part of the section is on the mechanical properties of such microimplants.

2.3.1 fabrication of microimplants

The main challenge in fabricating a chip-in-foil system is the electrical connection of the chip, which of course refers to a bare die. The chip-in-foil system consists of the die (or several dies) and the remaining foil-system which has to include the conducting tracks. This system can be fabricated on various foil materials using different fabrication techniques. The structuring of conducting tracks using sputter deposition, photolithography and dry etch is a possibility

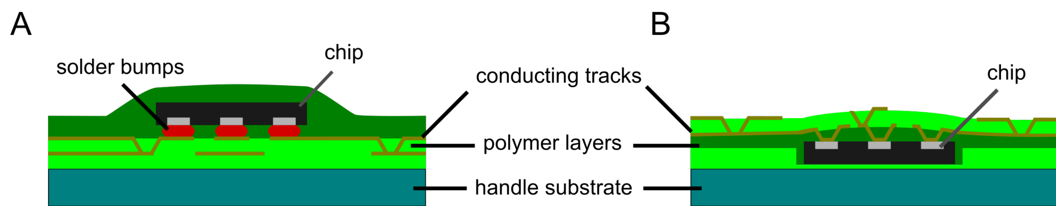


Figure 2.5: Sketch of the two main routes towards a chip-in-foil system. A: Chip is turned face-down and bonded to a prepared foil-system containing the conducting tracks. B: Chip is placed face-up and the topography is equalized in order to allow the fabrication of all conducting tracks on top.

providing excellent resolution. However, depending upon the size of the die and the system, other processes can also be used. Flexible electronics can be printed using different methods and materials [66]. The two main routes for the fabrication of the total system are either to fabricate the foil-system with all conducting tracks first and then place the die or rather the dies face-down on this system (Fig. 2.5 A). This requires then a flip-chip bonding process. However, all conducting tracks are in one plane and no topography has to be overcome. A face-up placement of the die/dies and the use of wire-bonding would result in very delicate electrical connection and is therefore not used. The other route for the fabrication is the face-up placement of the die/dies on a substrate and the fabrication of the conducing tracks directly on top of the die/dies. Therefore the topography due to the die/dies has to be compensated (Fig. 2.5 B).

Lee et al. developed a face-down interconnection process based on polymeric bumps that could be fabricated with a diameter of only $50\ \mu\mathrm{m}$ [67]. Compared to conventional face-down bonding using metal bumps their polymeric bumps are softer and allow the use of lower bonding temperatures and might thus result in lower stress concentration near bump and chip face.
Tokuda et al. used a flip-chip bonding process for the fabrication of a multichip neural stimulator [64]. They bonded using platinum bumps and the size of the bonded contact pads on the dies was about $80\ \mu\mathrm{m} \times 80\ \mu\mathrm{m}$.
Pothof et al. integrated CMOS chips thinned down to $40\ \mu\mathrm{m}$ into polyimide foil using flip-chip bonding [65]. Besides bonding, a biocompatible epoxy as underfill was used, increasing the bond strength.
For face-up processes the thickness of the dies to be embedded plays a key role. Leveling by spin coating a polymer layer on top of the die placed on a flat surface is a challenging task and requires a liquid polymer covering the step introduced by the die after spin coating. Furthermore a glue for gluing the die to the prepared substrate prior to the leveling process has to be compatible with the curing process of the liquid polymer spin-coated on top for the leveling.
Polyimide has been used as polymer for such a leveling process. Benzocyclobuten (BCB) was used to glue an ultra-thin CMOS die with a thickness of only $15\ \mu\mathrm{m}$ to a polyimide foil.

Polyimide[1] was then spin-coated on top of the die to a thickness of about $20\,\mu m$. After curing of the polyimide, laser drilling was used to open the polyimide on top of the dies contact sites [68]. A modified process using a photosensitive polyimide allowed the direct opening of the contact sites through illumination with a photomask [69].
The preparation of substrates with cavities can be a possibility to simplify the compensation of the topography introduced by the dies. Placing the dies into cavities reduces the topography that has to be leveled by filling up with material. However, it adds the step of preparing the cavities. The cavities can either be prepared from a flexible polymer remaining in the foil-system, or can be temporary requiring a procedure to detach the foil at the end. In both cases the polymer used for leveling has to accomplish a difficult task. In order to allow placement of the dies in the cavities they have to be slightly larger than the dies. Therefore, the polymer has not only to equalize the height difference due to a possible difference in cavity depth and die thickness, but also has to fill the remaining volume of the cavities. This requires good covering properties of the polymer. Further it can cause problems during curing of the polymer, especially if the curing comes along with the evaporation of solvent or gaseous reaction products, since where the polymer fills the gap between die and cavity the thickness of the polymer is as thick as the die.
Barz et al. introduced an embedding process for $50\,\mu m$ thick dies using shellac as a temporal filler for leveling [70]. The dies are placed upside down on a PDMS substrate and then spin-coated with a solution of shellac dissolved in ethanol. When the dies are completely covered by shellac a new glass substrate is bonded to the shellac, the sample turned around, and the PDMS removed from the surface of the dies uncovering a planar surface. Parylene C is then deposited on top, before standard lithographic procedures are used to structure conducting tracks. Finally the shellac is dissolved in ethanol revealing a thin parylene foil with the dies attached.

During fabrication the flexible systems are usually attached to a rigid handle substrate. For easy release of the completed foil-device sacrificial layers are favorable. The use of SiO_2 as sacrificial layer is a common choice, being etched with hydroflouric acid (HF). Aluminum and titanium can also be used as sacrificial layers, however the use of HF or other aggressive acids or alkaline solutions can be problematic due to their low selectivity or toxicity. Organic polymers such as PMMA (poly(methyl methacrylate)) or photoresists can be dissolved in organic solvents. However, the use of photoresists limits the maximum temperature of further process steps to temperatures before the photoresists starts to soften, deform and possibly flow away. Water-soluble sacrificial layers avoid any plasma oxidation or harsh chemicals. Among the materials used are: poly(acrylic acid) (PAA), poly(vinyl alcohol) (PVOH), dextran, sucrose and NaCl [71–73]. Some of these sacrificial layers do not react to the exposure of organic solvents, which can be a big advantage during surface micromachining. The etching rates reached for PAA and dextran in water are $750\,\frac{\mu m}{min}$ or $380\,\frac{\mu m}{min}$ respectively, and therefore more than two orders of magnitude higher than the etching rate of thermal SiO_2 in concentrated HF which is about $1.3\,\frac{\mu m}{min}$ [71].

[1]PI2611, HD MicroSystems

2.3.2 materials used for microimplants

The choice of materials has to consider the aspects of biocompatibility and biostability. Obviously no toxic materials should be used; this especially holds for flexible implants excluding rigid hermetic housings. The insertion of any implant comes along with traumata and inflammatory reactions [74]. The surface of the implant exposed to the body then determines the reaction of the surrounding tissue. Protein adsorption is the first step of any body response which might then trigger the formation of a stable encapsulation of fibrotic tissue [52, 74–76]. For electrically active implants such an insulating encapsulation is to be avoided. The substrate material and coating therefore must be chosen in a way minimizing the reaction after implantation. Cytotoxicity tests with standardized cell cultures are therefore used to investigate materials e.g. to see if toxic products diffuse out of the material [75]. However, biocompatibility is not only a question of surface chemistry and surface topography; the structural properties of the implant and thus of the used materials are also important [51,74]. Structural properties refers to weight, shape and Young's modulus of the implant having also high impact on the often soft surrounding of the implant [51]. For example for the bulk brain elastic moduli between 100 Pa and 10 kPa are typically reported [51]. The inability of a stiff device to follow naturally occurring movements can lead to chronic inflammation [51].

Besides the impact of the implant on the body, the body also has a high impact on the implant. The body is a harsh and aggressive environment for any implant and especially electrically active implants struggle with the high humidity. For conducting tracks therefore noble metals such as gold or platinum should be chosen.

As base material for flexible implants different polymers have been used. Interesting properties besides biocompatibility and biostability are Young's modulus, electrical insulation as well as available manufacturing technologies and handling properties.

The most widely used class of polymers are silicones with polydimethylsiloxane (**PDMS**) being the most common one [77]. PDMS has good biocompatibility and a low Young's modulus allowing the fabrication of flexible and stretchable devices. Silicones in general are highly permeable to gases and vapors, including water [52, 77]. There are different cross-linking processes that can be used to transform the liquid PDMS into a soft elastomer. The most common are cross-linking with radicals, cross-linking by condensation and crosslinking by addition [77]. PDMS can be processed using spin coating with layer thicknesses in the range of about $10\ \mu m$ to about $100\ \mu m$ in reach, but can also be used in a molding process. Curing can be performed at room temperature.

There are many medical grade silicones on the market that are approved by the United States Food and Drug Administration (FDA).

A PDMS widely used for the fabrication of systems on the microscale is the two component PDMS Sylgard 184[2]. While it is not sold as medical grade its properties have been well examined due to its prevalent use in research. The two components do not include any solvent so there is no degassing during curing. Shrinkage during curing depends on curing temperature and is about zero for curing at room temperature [78]. Curing at higher temperature goes much faster and takes only about 40 minutes at 120°C but is then accompanied by shrinkage of about

[2]Dow Corning, Midland, USA

$2.7\,\%$ [78]. The mechanical properties can be changed by modifying the mixing ratio of the two components, but they also depend on the curing temperature [79]. For the recommended mixing ratio of $10 : 1$ (base : cure) cured at room temperature Young's modulus is about $1.32 \pm 0.07\,$MPa [79].
Another class of polymers that has been used for flexible implants are **polyimides**. Polyimides provide high dielectric strength, low moisture absorption and high temperature stability [52]. However, while foils made of polyimide are flexible they are not stretchable. The processing is done using spin coating, resulting in thicknesses between $1\,\mu m$ and $15\,\mu m$ in a single step. Afterwards a curing step at a temperature of $\approx 350°$C in nitrogen atmosphere is required. While there is no polyimide approved by the United States Food and Drug Administration (FDA) its biocompatibility and low cytotoxicity has been shown [80].
Another class of polymers that has been used for flexible implants are parylenes (poly-paraxylylene). The different parylenes provide a wide range of properties ranging from high chemical inertness to solvent solubility [81]. **Parylene C** is the most popular parylene for biomedical applications and has shown good biocompatibility. Parylene C is certified according to *ISO 10993* and approved for permanent implantation by the United States Food and Drug Administration (FDA) [52, 81]. It provides high dielectric strength and low moisture absorption [52]. Deposition is performed in a room temperature CVD process in vacuum, in which the parylene C condenses on the surface of the samples. Thus, the deposition process is conformal meaning the parylene covers the complete surface independent of its complexity and thus there is no equalizing effect in surface topography. Possible thicknesses are $1\,\mu m$ to $100\,\mu m$. Due to its chemical inertness the adhesion of parylene C is poor, but is significantly increased to silicon and silicon compounds using the silane A-174 (methacryloxypropyl trimethoxysilane) as adhesion promoter.

2.3.3 failure of microimplants

The reasons for an implant to fail are manifold. As stated above the body might encapsulate the implant with fibrotic tissue. This encapsulation increases the distance to the targeted tissue and can prevent the implant from performing its desired function, while in principal its technical functioning is still given. This kind of failure has to be addressed by proper design of the device concerning its materials and surface properties.
In this section those kind of failures shall be discussed that affect the technical functioning of the implant. A source of failure sometimes overseen is the handling of the implant prior and during implantation. This can mean strong mechanical load on the device, coming along with bending – and thus stretching or compression of different material layers – in flexible devices. For chip-in-foil systems consisting of different polymeric layers with layers of metallic conducting tracks in between and embedded dies there are several boundaries where the elastic modulus changes. These positions can build preferential breaking points. Their occurrence and effect will be discussed in more detail in the next section.
In the body the implanted device might face further mechanical load, due to movement of the surrounding tissue. This can lead to accelerated aging of layers within the system that are less mechanically robust or brittle.

The biggest cause for failure is the humid environment in the body. Water is an excellent solvent and catalyst for different failure mechanisms. Corrosion of conducting tracks in electrically active implants can occur when tracks with different electrical potentials are connected through a conducting water film, but also the contact of different metals can boost corrosion [82]. Surface migration of metal ions can lead to the growth of solid metal lines (sometimes referred to as whiskers or dendrites) between two tracks at different electrical potentials until a short circuit occurs [82]. This effect depends on the metal used for the tracks. While silver, copper and aluminium start to migrate in distilled water, gold and platinum only migrate in the pressence of ions [83]. Hence, conducting tracks should be fabricated from gold or platinum, while aluminum and copper as well as the presence of too many different metals should be avoided. CMOS dies embedded into the system are also very sensitive to ions dissolved in liquid water. Observations inidcate, that ions can diffuse through the protective coatings around a CMOS device and change the p-n junctions and thus the behavior of the implemented circuit [84, 85]. Also corrosion of the insulating material between the conducting tracks can cause failure [82].
In order to avoid failure due to these mechanisms the presence of condensed water inside the implant should be prevented. Flexible implants – contrary to the use of a hermetic housing – therefore can follow three ideas. Water is only problematic in its liquid form and the water uptake of the polymeric base material of the flexible system by itself is not a problem. Thus, water vapor should not condense in any voids inside the implant [85]. The first idea is thus to prevent the condensation of liquid water inside the implant. The second idea is to hinder water intrusion with barrier layers. As the device is flexible those barrier layers can only be inorganic thin-films. The third idea is a variant of the second idea and aims not for an impermeable barrier, but for a deceleration of water permeation. Delaying water intrusion can retard the start of corrosion and thus allow a sufficient lifetime of the implant of possibly weeks instead of minutes.
Different polymers come along with very different water permeabilities and ionic permeabilities. For example for the ionic permeability of polyimide the diffusion coefficient has been determined to be $-0.2 \cdot 10^{-15}\,\frac{\mathrm{m}^2}{\mathrm{s}}$, while for polyamide its value was determined to be $-1.6 \cdot 10^{-15}\,\frac{\mathrm{m}^2}{\mathrm{s}}$ [86]. A possible mechanism that could lead to failure of an implant made of polymer foils is the formation of an osmotic pressure pulling water inside the implant once water has condensed inside the implant and dissolved ions from a surface, interface or contamination. Hence, using a polymer that is a good ionic barrier and avoiding contamination and defects inside the implant (where ions might dissolve) could result in the opposite case, where the osmotic pressure drives the water out of the implant towards the body electrolyte, which contains many ions. However, avoiding any defect or contamination is almost impossible. Flexible chip-in-foil devices are multilayer systems with many interfaces. Poor adhesion between different layers can lead to delamination of different layers. With the device decomposing short circuits can directly occur and a failure of functionality is likely to appear.
So following the first idea, good adhesion between the different layers and materials of the implant is the key characteristic for longtime stability in wet body environment. Particularly the adhesion of metals on polymers usually is bad. To increase adhesion surface pretreatments can be conducted. Plasma is a possibility enabling cleaning of the surface (e.g. Ar, O_2) and

change of the surface chemistry (e.g. O_2, N_2, H_2). The formation of hydroxyl (–OH), carbonyl (C=O) and carboxyl (COOH) groups can enable the formation of covalent bonds and thus, increase adhesion [87]. The use of additional adhesion promoting layers is another possibility to increase the adhesion between different materials. Silanes are predestined to promote adhesion between polymers and inorganic materials [88].

Following the second and third idea additional layers with low water permeability can be deposited as barrier hindering water diffusion into the implant. As the vulnerability of the flexible implant arises from the high water permeability of polymers, those barrier layers should be made of inorganic materials e.g. metals or metal oxides [89]. The amount of defects in the barrier layer is then crucial to its effect. For a stack of several barrier layers also the adhesion between these layers is of relevance. Pores in two neighboring layers are unlikely to be on the exact same position and so diffusion through a pinhole will stop at the next layer. However, in the case of poor adhesion, the water diffusing through a pinhole in the first layer will condense in cavities at the interface allowing lateral movement of the water, enabling then the diffusion through pinholes in the second layer [90]. It has been shown that permeation through a metal oxide barrier layer from a critical thickness on does not depend on layer thickness, because it is dominated by diffusion through defects as pinholes [91]. It is thus important to deposit layers with low defect density. Therefore, atomic layer deposition – providing high quality films with low defect density – is used. The deposition of multilayers is a possibility to lower the impact of defects. Diffusion paths through pinholes in a layer stop at the next layer where the water has to diffuse through the layer material until it reaches another pinhole. Another effect that can help to increase the barrier properties of multilayers composed of alternating polymeric and inorganic layers is a smoothing effect due to the polymer improving the likelihood of depositing one 'perfect' layer [92]. However, it has also been stated out that the tremendously extended diffusion path for the water only results in a delay until an equilibrium is reached. Therefore, it might be that some of the reported values for the water vapor permeation of multilayers might not be steady-state values if the measurement time was too short and thus, the real values might be much higher as reported [93]. Yet, the use of multilayers is still a useful path towards a stable implant and corresponds to the above mentioned third idea. Depending on the required lifetime of the implant, it can be sufficient to slow down the water intrusion.

One big issue of these barrier layers arising is their limited mechanical robustness. While metal oxides as Al_2O_3 have low water vapor permeability and are electrical insulating, they are also brittle and thus their use on a flexible system is problematic [92]. Thus, the exact composition of the chip-in-foil system with its different material layers including brittle barrier layers has to be well considered. The mechanical properties of chip-in-foil systems consisting of multiple layers with different properties – as the device envisioned within this work – are therefore discussed in the next subsection.

2.3.4 mechanical properties of microimplants

Foil systems consisting of layers of different materials face stress due to external bending and internal stress of the individual layers resulting from the deposition process. The different components of the system are:

- polymeric layers,
- dies embedded in the polymer,
- conducting tracks,
- barrier layers against water vapor intrusion.

The polymeric layers build the basis of the foil and primarily determine the mechanical properties of the total system. The polymers come along with low Young's moduli enabling flexibility (and probably stretch-ability) of the device. The dies embedded in the polymer occupy a notable volume of the device at their location in the system. As the Young's modulus of silicon is about 10^3 to 10^5 times the Young's modulus of polymers it has also great influence on the flexibility of the total system. This holds also for the case of ultra-thin dies that become bendable [94].
The conducting tracks neither cover the complete surface, nor do they cover any major continuous area as e.g. the dies do, thus their influence on the mechanical properties of the system is reduced. However, as they are essential for the functioning of the device their mechanical ruggedness is of high relevance. Conventional metal conducting tracks for example are only stretchable to a very low degree.
Barrier layers, added to the system to protect the system from water vapor intrusion, consist mostly of brittle materials. Any crack formation due to stress – terminating its function as barrier – would make their presence obsolete.
The internal stress of thin films consists of a part due to different coefficients of thermal expansion α_i and deposition at elevated temperature and intrinsic stress originating from the layer formation process [95]. The thermal stress for a layer i is $\sigma_T = \Delta T \cdot \alpha_i \cdot E_i$ with the Young's modulus E, and thus it increases with increasing temperature difference ΔT between substrate temperature during deposition and temperature during usage. The intrinsic stress strongly depends on the conditions during deposition (e.g. substrate temperature and deposition rate) [95–97]. Intrinsic stress arises from different processes during film growth, when the atoms condense on the surface and rearrange. The coalescence of grain boundaries is one example for a mechanism leading to tensile stress. Intrinsic stress can be tensile or compressive and is typically in the range of 0.1 to 3 GPa [95,96]. For 100 nm thick layers of Al_2O_3 deposited using atomic layer deposition values for intrinsic in-plane stress between 383 and 474 MPa (tensile) have been reported [98]. For a 150 nm thick platinum layer deposited using e-beam evaporation tensile internal stress of ≈ 230 MPa (for a deposition rate of 0.1 nm/s) has been reported [99]. In contrast for parylene C a compressive internal stress of only 6 MPa after deposition has been reported [100].
Films with high internal stress can lead to a warpage or roll-up of the complete layer system, if they are not balanced.
Thin films are sensitive to any strain. While gold films on a soft substrate start to fail at 3% strain, brittle films as they might be used for water vapor barrier layers (e.g. Al_2O_3) start to fail below 1% of strain [92]. Failure occurs due to the growth of microcracks, film cracking (channeling) and debonding [92]. For conducting tracks this first leads to increased track resistance and then to rupture of the track. The cracking of barrier layers opens new diffusion

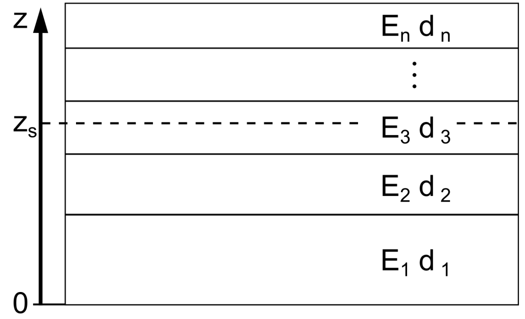


Figure 2.6: Schematic showing a multilayer system with layers 1 to n with thicknesses d_i and Young's moduli E_i.

paths for water vapor and thus increases the water vapor transmission rate (WVTR) of the barrier. Cracks also lead to a redistribution of shear stresses and thus can have catastrophic impact on the devices stability [95]. A substrate with higher elastic modulus can lead to more uniform deformation and thus gold films deposited on polyimide can survive strain $> 10\%$ [92]. The stress σ and strain ε due to external bending can be modeled using beam-bending theory [101]. Therein, a linear stress-strain relationship $\sigma = \varepsilon \cdot E$ is assumed. Also all crosswise working forces are neglected. The system consists of n layers with thicknesses d_i and Young's moduli E_i (Fig. 2.6). As rectangular cross-section with width b is assumed, the cross-sectional areas $A_i = b \cdot d_i$ can for simplicity be replaced by the layer thicknesses d_i.
There is then a plane – parallel to the surface of the beam – that faces no strain, when the beam in bent. This plane is called the "zero-strain plane". In the simplified model neglecting any two-dimensional expanse it comes down to an axis. If there is no internal stress the zero-strain axis or neutral axis coincides with the zero-stress axis [102]. Its position from the surface of layer 1 can be calculated using:

$$z_1 = \frac{\sum\limits_{j=1}^{n} d_j E_j \left(\sum\limits_{n=1}^{k-1} d_n + \frac{d_j}{2} \right)}{\sum\limits_{i=1}^{k} E_i d_i}$$

with $d_0 = 0$. For a bi-layer system the equation becomes:

$$z_1 = \frac{d_1^2 E_1 + d_2 E_2 (2d_1 + d_2)}{2(d_1 E_1 + d_2 E_2)}.$$

The system of total thickness $d_1 + d_2$ is then divided into a part z_1 with positive stress and strain, and a part $z_2 = d_1 + d_2 - z_1$ with negative stress and strain. From geometrical considerations it is obvious, that the strain changes linearly through the cross-section. It is zero at the neutral axis at $z = 0$, $\varepsilon_{\text{max1}}$ on the surface of layer 1 ($z = z_1$) and $-\varepsilon_{\text{max2}}$ on the surface of layer 2 at $z = -z_2$ (see Fig. 2.7 right). It is then easy to derive the relation:

$$\frac{\varepsilon_{\text{max1}}}{z_1} = \frac{\varepsilon_{\text{max2}}}{z_2},$$

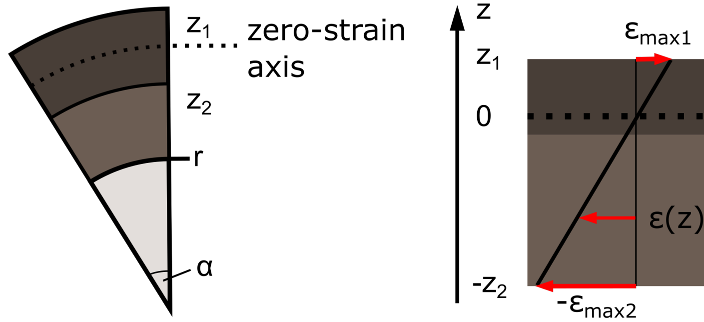


Figure 2.7: Left: Schematic of a segment of a bi-layer system under bending. Right: Schematic of the strain distribution in a bi-layer system.

from which an expression for the strain at any position z within the layer-stack can be derived:

$$\varepsilon(z) = \frac{\varepsilon_{\text{max1}}}{z_1} \cdot z.$$

The absolute values of the strain on the upper and lower surface of the layer system are therefore not the same.
The same results can be obtained by calculating the moment above and below the neutral axis, which have to be equal in absolute values but opposite in sign.

$$M_{\text{above}} = \int_0^{z_1} E_1 \varepsilon_{\text{max1}} \frac{\tilde{z}}{z_1} \mathrm{d}\tilde{z} = \frac{1}{2} z_1 E_1 \varepsilon_{\text{max1}}$$

$$M_{\text{below}} = \int_{z_1-d_1}^{0} E_1 \varepsilon_{\text{max2}} \frac{\tilde{z}}{z_2} \mathrm{d}\tilde{z} + \int_{-z_2}^{z_1-d_1} E_2 \varepsilon_{\text{max2}} \frac{\tilde{z}}{z_2} \mathrm{d}\tilde{z} = -\frac{1}{2} \frac{z_1^2}{z_2} E_1 \varepsilon_{\text{max2}}$$

As $M_{\text{total}} = M_{\text{above}} + M_{\text{below}} \stackrel{!}{=} 0$ this leads to the same relationship between $\varepsilon_{\text{max1}}$ and $\varepsilon_{\text{max2}}$ as above. Alternatively the expression can be used to calculate the position of the neutral axis.
A relation between strain and bending radius r can be derived looking on a little segment of the bent system (Fig. 2.7 left). The opening angle of the circular segment is:

$$\alpha = \frac{360° \cdot L_0}{2\pi(r + z_2)} = \frac{360° \cdot (1 - \varepsilon_{\text{max2}}) L_0}{2\pi r} = \frac{360° \cdot (1 + \varepsilon_{\text{max1}}) L_0}{2\pi(r + d_1 + d_2)}.$$

The first term corresponds to the position of the neutral axis, the length of the segment (the arc length) is L_0. The second term corresponds to the position on the lower surface, where the segment is compressed and thus $L = L_0 - \Delta L = (1 - \varepsilon_{\text{max2}}) \cdot L_0$. The last term corresponds to the position on the upper surface, where the segment is stretched by a factor $(1 + \varepsilon_{\text{max1}})$. It then holds:

$$\varepsilon_{\text{max1}}(r) = \frac{r + d_1 + d_2}{r + z_2} - 1$$

$$\varepsilon_{\text{max2}}(r) = 1 - \frac{r}{r + z_2}.$$

While the strain changes linear above the stack, the stress is not continuous between different material layers. This then leads to shear forces between the layers [101].
If internal stress is added to the model, the zero-strain and zero-stress axis are not the same [102, 103]. While there is still only one zero-strain axis, there can be several zero-stress axes.

2.4 transfer and assembly methods

For the fabrication of the envisioned device a transfer and an assembly process are crucial, in particular when looking on the cost efficiency of the process. While the spacing of the dies in the desired array is about $1\,\text{mm}$ they will be fabricated on the wafer as closely packed as possible. Also for the further fabrication the dies for one array have to be transferred to another substrate, as the envisioned device covers a larger array than just the die array.
There are then two basic approaches to handle this issue. The first is to completely separate the dies to a loose mass of dies that in our case would basically look like sand. From there on sophisticated processes would sort, orient and transport the dies before finally assembling them in the given way. The second approach – which is currently more popular – is based upon processes completely conserving the order of the dies as given on the wafer. The idea is then, as it is too difficult to arrange dies with such a high accuracy as given on the wafer after fabrication this order should never be abandoned.
The dies for the device envisioned within this work are $250\,\mu\text{m} \times 250\,\mu\text{m}$ in size with a thickness between $150\,\mu\text{m}$ and $250\,\mu\text{m}$ and have contacts with a pitch of $40\,\mu\text{m}$ on their surface. This contact pitch determines the required relative placement accuracy of the individual dies within the array and therefore the required assembly and transfer process has to work on the mesoscale connecting the microscale (contact pitch on top of the individual dies) with the macroscale (die pitch in the array).
This section gives an overview on different assembly methods distinguishing between serial and parallel and between deterministic and stochastic processes. It then presents different concepts for picking micro devices, which is a central problem to all deterministic processes. In the last subsection transfer printing as a deterministic parallel assembly procedure is discussed in detail, as it was chosen as the most suitable method for the fabrication of the envisioned device.

2.4.1 assembly methods

The high number of different assembly methods can be divided into serial and parallel processes [104]. Parallel processes can either be deterministic or stochastic [104].
The assembly process is the link between the fabrication of the individual parts and the fabrication of new complex systems including those parts. Therefore, the way in which the parts to be assembled are supplied plays a key role for the process. This can for example include the separation process of devices fabricated in a wafer batch process. The choice of the best method for a certain assembly task depends on different conditions:

- the size, shape, and number of the parts to be assembled
- the presence of different non-identical parts
- the relevance of the orientation of the parts
- the pattern the parts have to be assembled (e.g. regular array or special layout)
- the required accuracy

Serial assembly processes assemble one piece after the other. The simplest process is assembly by hand. The use of a microscope and tweezers allow the handling of parts with sub-millimeter size with high accuracy. However, speed and achieved accuracy highly depend on the individual concerned.
Serial assembly normally is known as "pick and place" and is a deterministic procedure. The capabilities of "pick and place" concerning the size and shape of the parts that can be assembled depend on the individual solution for grasping the parts implemented in the system. The number of parts directly transfers to the time required for the assembly. "Pick and place" however is the most flexible assembly procedure and can pick up different parts from different sources. Also it can place parts in each desired pattern. Accuracy again depends on the individual system.
A "pick and place" system requires a solution for picking, manipulating and placing the devices and an accurate positioning system.
Visual systems are used to gain optical feedback and increase the accuracy [105]. The system presented by Tamadazte et al. reaches a placement accuracy of $1.4\ \mu m$ and an orientation error of only $0.5°$ [106]. The assembly of surface-mount devices (SMD) on printed circuit boards is a task were automated "pick and place" is performed with device sizes of $0.6\,mm \times 0.3\,mm$ (0201 metric packages) using automated machines. The SIPLACE TX series[3] allows the assembly of parts with sizes down to $0.12\,mm \times 0.12\,mm$ with a placement accuracy of $25\ \mu m$.
Parallel assembly processes assemble ensembles consisting of a high number of parts simultaneously. Parallel assembly can either follow a deterministic or a stochastic approach [104]. Deterministic parallel procedures can be a modified "pick and place" where the picking tool is capable of transferring several parts at once [107]. Then there are wafer-to-wafer transfer procedures, where parts fabricated on one wafer are transferred to a second wafer using bonding processes [104]. There is then no transferring tool necessary temporarily holding the micro-devices. Separation of the parts from the first wafer can be enabled by sacrificial layers or the parts only being held by anchor structures. These procedures are mainly transfer procedures, and allow only little change concerning the assembly of the parts from their initial arrangement. The use of selective transfers, transferring only a chosen subgroup of the parts allows for example a change in the spacing of neighboring parts.
Stochastic procedures are suitable for assemblies of 10^6 or more elements and can be very fast. They follow the aforementioned second approach towards the desired assembly by giving up any pregiven order. To enable self-assembly the parts are for example dispensed in a solution allowing them to move randomly [108]. Ultrasonic vibration is an alternative source of random kinetic energy [104]. The assembly is achieved by preparing the substrate in a way that the

[3] ASM Assembly Systems GmbH & Co. KG, Germany

desired assembly state forms a minimum in potential energy [104]. This can be achieved by preparing specific binding sites or traps like little cavities, where the randomly moving parts are caught. In the case of little cavities matching the size and shape of the parts gravity assembles the parts due to the difference in density between parts and fluid [108].
The accuracy of the assembly then strongly depends on the accuracy of the fabrication process used to prepare those traps e.g. photolithography.
For stochastic processes the assembly of symmetric parts requiring specific orientation is challenging. For example for little dies in the shape of small cubes ($250\ \mu m \times 250\ \mu m \times 250\ \mu m$) caught in cavities there are for each die six possibilities which surface of this cube will be on top, and for each case there are four different possible orientations. So on average only one in twenty-four dies would be oriented in the desired way.
A concrete example for a complete self-assembly process meeting also the requirements in this work was developed in the project "FluidAssem" [109]. The parts were dispensed in water and fed through channels. Surface tension holds the parts on the surface of the water and sophisticated procedures can be used to first row all parts up in a single line, allowing then sorting or manipulation of the individual parts prior to assembly. The individual parts were then transported to an edge were they fell to a prepared hydrophobic substrate with hydrophilic areas at the desired positions for the parts.
Each hydrophilic area had the size and shape of one element to be assembled and water droplets for catching the elements were placed on top of these areas. Due to the different hydrophilic and hydrophobic areas the droplets move to the correct position above the hydrophilic area in about 20 ms if they are not placed correct in the first place [110]. The parts were then dropped to these water droplets. Once caught by a droplet surface tension lead to a self-centering process resulting in a placement accuracy better than $10\ \mu m$ [110].
Following a similar approach using surface tension and capillary forces for a self-alignment of parts by modulating surface hydrophobicity Xiong et al. have developed a multibatch self-assembly process and demonstrated a two batch micro assembly [111, 112].

2.4.2 gripping micro-devices

Different physical principles can be used for gripping micro-devices. Tichem et al. name different micro-grip principles and make an approach to classify them (see Fig. 2.8) [113]. Micro-grip principles that have been used are:

- friction in friction-based gripping
- form closure in gripping
- suction as in a vacuum tool
- magnetism
- electrostatic forces
- surface tension and capillary force due to a liquid between gripper and the parts
- van der Waals forces

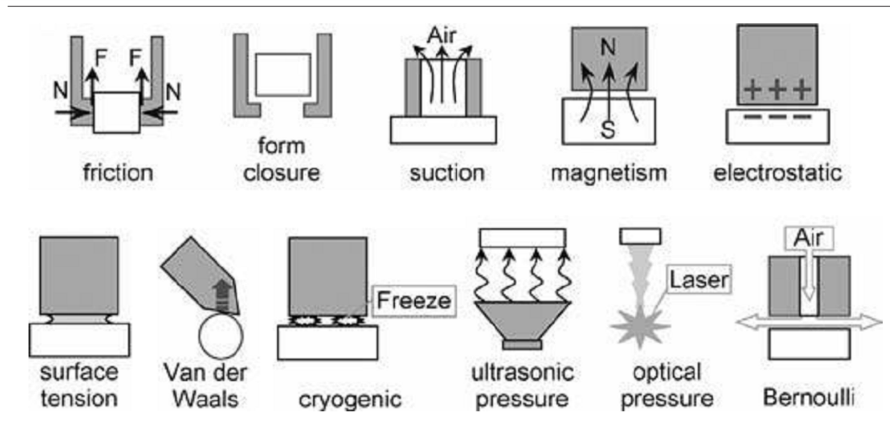


Figure 2.8: Sketches of different micro-grip principles. (taken from [113])

- cryogenic gripping, where a small amount of liquid is frozen between the gripper and the part
- ultrasonic pressure
- optical pressure, as in optical tweezers
- Bernoulli effect resulting in an under pressure due to air flow between gripper and part

Gripping devices becomes more challenging as devices get smaller. The reason is the different scaling of the forces involved [105, 114–116]. The size of a system could be described by a scaling factor s. Initially $s = 1$, but for $s = 0.1$ each dimension of the system is decreased by a factor of ten. Different variables then scale differently. While a simple length scales $\left[\ s\ \right]$, an area scales $\left[\ s^2\ \right]$ and a volume $\left[\ s^3\ \right]$. Assuming that density does not change with size the mass of objects then also scales $\left[\ s^3\ \right]$.
According to W. S. N. Trimmer [114] there are then several possibilities how different forces might scale with size: $F = \begin{bmatrix} s \\ s^2 \\ s^3 \\ s^4 \end{bmatrix}$. As $a = \frac{F}{m}$ the acceleration scales with $a = \begin{bmatrix} s^{-2} \\ s^{-1} \\ s^0 \\ s^1 \end{bmatrix}$ and the time for things to happen which is $t = (\frac{2x}{a})^{1/2} = (\frac{2xm}{F})^{1/2}$ scales as $t = \begin{bmatrix} s^{1.5} \\ s^1 \\ s^{0.5} \\ s^0 \end{bmatrix}$. It is then interesting to examine which force scales how. Forces scaling with s^3 or s^4 will lose importance in comparison to forces scaling with s^1 or s^2. The gravitational force between two bodies of mass m_1 and m_2 separated by a distance r_{12} as given by Newton's law of gravitation is $F_G = \mathrm{G}_0 \cdot \frac{m_1 m_2}{r_{12}^2}$ with G_0 the gravity constant. The gravity force then scales $\left[\ s^3\ \right]\left[\ s^3\ \right]\left[\ s^{-2}\ \right] = \left[\ s^4\ \right]$ and thus is insignificant when going to the microscale. However, more important when handling micro objects is the gravitational force due the mass of the earth,

which is not scaled down. $F_g = m \cdot \mathrm{g}$ with $\mathrm{g} \approx 9.81\,\frac{\mathrm{m}}{\mathrm{s}^2}$ and m the mass of our micro object scales with s^3. Pneumatic and hydraulic forces caused by pressure scale with s^2. Surface tension depending on the contact length scales with s^1 [114].
Generally adhesion forces are proportional to surface area. They can be due to electrostatic forces arising from charge generation or charge transfer during contact, van der Waals forces, or surface tension when moisture has adsorbed to the two surfaces [114, 117]. R. S. Fearing [114] states that as surface tension requires a fluid layer, and van der Waals forces are only significant for gaps less than about $100\,\mathrm{nm}$ – requiring smooth surfaces – electrostatic forces are most relevant. He calculates the edge length l of the smallest silicon cube that will not stick to a surface due to electrostatic forces, assuming a maximum charge density of $3 \cdot 10^{-5}\,\frac{\mathrm{C}}{\mathrm{m}^2}$ due to the breakdown strength of air and centimeter size gaps. As result he gets a minimum size for the cube of $2\,\mathrm{mm}$.
So, while it is possible to built **miniature grippers** [107, 118, 119] the different scaling of adhesion and gravitational force lead to new effects. For parts with masses of several grams gravitational force dominates adhesive forces and when the gripper opens the part will drop [115]. For parts of less than 1 gram mass, picking, moving and placing come along with effects due to adhesion. During picking electrostatic attraction may cause the part to jump off the surface adhering to the gripper depending on an initial charge distribution. During placement gravitational force is not strong enough to pull the part from the gripper, and thus the part will stick to the gripper unless the adhesion between part and surface exceeds the adhesion between gripper and part. Handling thus requires dedicated planing and strategies, where the movements for picking and placing differ [120].
In order to reduce adhesion effects material choice and geometry are essential. Contact electrification should be minimized and a conductive material used. A rough surface of the gripper reduces contact area, while a hard material prevents local deformation increasing the contact area [115]. A dry atmosphere helps to reduce surface tension effects [115]. However, an alternative would be the assembly within a fluid eliminating electrostatic and surface tension effects [115].
Besides mechanical grippers **vacuum tools** are an often used method for picking devices. The contact pressure σ holding a device of mass m can be written as $\sigma = \frac{F - m \cdot (\mathrm{g}+a)}{A_{\mathrm{grip}}}$ with the holding force F, the acceleration a of the handling machine and the gripping area A_{grip}. The holding force F is

$$F = (p_{\mathrm{atm}} - p_{\mathrm{vac}}) \cdot A_{\mathrm{suc}} \cdot \eta \cdot \gamma$$

with η being an efficiency factor due to leakage of the vacuum system and γ being a factor < 1 including deformation of the vacuum tool leading to a smaller effective force interaction area. So the effective pressure difference Δp of the vacuum gripper is $(p_{\mathrm{atm}} - p_{\mathrm{vac}}) \cdot \eta$ [121]. Typically a pressure difference Δp of about 0.91 bar is reached [121]. The force interaction area A_{ia} – the area on the part exposed to the underpressure – is $\gamma \cdot A_{\mathrm{suc}}$ and thus smaller than the area A_{suc} surrounded by the vacuum seal of the tool. This area is of course smaller as the gripping area A_{grip} covered by the gripping tool, as the vacuum seal covers part of the area. The area A_{grip} can at maximum be the geometrical surface area of the device.
Gripping micro devices with vacuum tools is possible, as shown for example by Zesch et al. using an optimized glass pipette as vacuum tool to manipulate diamond crystals with a size of

only $100\,\mu m$ [122].
Picking up micro-devices strongly depends on the donor-substrate providing the parts. This does not have to be the substrate the parts are fabricated on, but for deterministic procedures conserving the initially given order from the fabrication, they have to sit in an ordered and secure way on a substrate. One common possibility is the parts being attached on an adhesive tape after separation using dicing or dicing before grind. Another possibility is the parts being lose except for some anchor structures holding them in their position on the substrate, that can be broken easily to pick up the part [94].

2.4.3 transfer printing

Transfer printing refers to a transfer procedure for transferring micro- and nanomaterials, including micro-devices, from one substrate to another using a stamp [123]. In terms of conventional printing techniques the micro-devices replace the ink. Three modes of transfer printing are possible. In additive transfer a material layer is prepared on top of the stamp and then corresponding to the stamps profile selectively transferred to a new substrate. Subtractive transfer refers to a process where a stamp is used to selectively retrieve the “ink” from a substrate. Finally there is deterministic assembly, where the stamp is used to selectively transfer “ink” from one substrate to another. This includes then two separate transfer steps for “inking” (transfer substrate to stamp) and “printing” (transfer stamp to substrate) [123].
Transfer printing is an adhesion based process that can be realized by implementing an adhesion cascade. The adhesion between stamp and “ink” has to exceed the adhesion between donor substrate and “ink”, while the adhesion between “ink” and receiving substrate has to exceed the adhesion between stamp and “ink”. The use of sacrificial layers and glue is a possibility to realize a successful transfer printing process. The stamp can be casted from PDMS. While PDMS comes along with low surface energy its softness allows it to establish good surface contact resulting in good adhesion due to van der Waals forces. The adhesion properties of differently shaped PDMS surfaces have been examined in detail in order to understand and imitate the adhesion of gecko feet [124–126]. Paretkar et al. measured the pull-off strength of PDMS fibrils in dependence of their aspect ratio and tip shape [127]. They used Sylgard 184[4] as PDMS and measured the pull-off strength with a separation speed of $10\,\mu m/s$, resulting in a pull-off strength for flat PDMS of about 0.035 MPa [127].
However, different efforts to control the adhesion of the stamp have been done, superseding the need for an adhesion cascade. Kim et al. fabricated stamps with micro-tips in the four corners of the flat surface [128]. For picking up a device the stamp is brought to contact with a high preload compressing those tips. The stamp is then in contact with the part with its whole area. After fast retracting the stamp with the device attached, the elastomer of the tips is allowed to relax, while the stamp is moved to its target position. This leaves contact between stamp and device only on the four micro-tips. So adhesion between stamp and device in low, when the device is brought into contact with the receiving substrate at low preload. Another approach towards an adhesion control of the stamp is the use of shape memory material for the stamp [129, 130]. Control of

[4] Dow Corning, Midland, USA

the stamps temperature can then be used to switch between a high contact state resulting in high adhesion and a low contact state with low adhesion.
A sophisticated solution for adhesion control is the exploitation of the viscoelastic properties of the PDMS allowing kinetic control of the stamps adhesion [123, 131, 132]. Viscoelastic properties imply a mix of elastic and viscous properties. Viscoelastic materials dissipate energy when load is applied and thus the stress-strain curve of an viscoelastic material shows a hysteresis. The separation processes in a transfer printing process (between substrate and part or stamp and part) can be modeled as the initiation and propagation of interfacial cracks [123,131]. The individual interfaces come along with characteristic energy release rates G for the breaking of interfacial bonds. The energy release rate is $G = \frac{F}{w}$ with F being the peel force applied in normal direction and w the width [133]. As substrate and part are considered to be elastic the critical energy release rate for the separation of their interface $G_c^{\text{part/substrate}}$ is considered to be a material property of the interface that does not depend on the peeling velocity v. For separation of the viscoelastic stamp from the part the energy release rate $G_c^{\text{stamp/part}}$ also accounts for viscoelastic energy dissipation around the crack tip propagating with the peeling velocity v [131]. Because the energy dissipation in the viscoelastic stamp increases with the peeling speed the energy release rate depends on the peeling velocity: $G_c^{\text{stamp/part}} = G_c^{\text{stamp/part}}(v)$ [131, 134–136]. For a transfer printing process two cases have to be realized. For picking up parts $G_c^{\text{part/substrate}} < G_c^{\text{stamp/part}}(v)$ has to be fulfilled while for printing $G_c^{\text{part/substrate}} > G_c^{\text{stamp/part}}(v)$ must be fulfilled [131].
From $G_c^{\text{part/substrate}} = G_c^{\text{stamp/part}}(v_c)$ the critical separation velocity v_c can be derived. When the stamp is detached with a speed $v > v_c$ the adhesion between stamp and parts exceeds the adhesion between part and substrate and the part is picked up. For a separation speed $v < v_c$ the adhesion between stamp and part is less than the adhesion between substrate and part and the part is printed to the substrate.
Successful printing of different objects including LEDs with a size of $200\ \mu\text{m} \times 200\ \mu\text{m}$ using kinetic control has been demonstrated [132, 137].
The transfer printing process with kinetic control of adhesion is protected by an US patent [138] and commercially used by the company “X-Celeprint” (Cork, Ireland).

2.5 atomic layer deposition

Atomic layer deposition (ALD) is a modified chemical vapour deposition (CVD) method developed independetly twice. In the 1960’s the “molecular layering” was invented in the Soviet Union, then in the 1970’s it was invented a second time in Finland under the name “atomic layer epitaxy” (ALE) [139]. The primary field of application for ALD is semiconductor device fabrication, where ALD layers are used as gate oxides, copper diffusion barriers or high-k dielectrics [140, 141]. An emerging field of use is the deposition of low gas permeability barriers [141, 142] or the use as corrosion protection [141, 143].
This section starts by giving a brief summary of different deposition methods developed before it introduces the ALD deposition method. It then points out the unique characteristics of the ALD deposition method. Different types of ALD are then presented. The last part of the section

focuses on the electrical properties of thin Al_2O_3 and TiO_2 films deposited with ALD and the use of ALD layers as water vapor diffusion barriers.

2.5.1 vapor deposition methods

Coatings are essential for numerous applications. For example optical coatings are used as reflective or anti-reflective coatings, while protective coatings aim for wear resistance or the prevention of corrosion. Deposition can be performed starting from the gas phase, from a liquid (e.g. spin coating or painting) or a solid (e.g. powder coating).
For the deposition of thin films from the gas phase many different methods have been developed that can be categorized into physical vapor deposition (PVD) and chemical vapor deposition (CVD). As the name already suggests PVD bases on physical processes, where the material goes from its condensed phase to a vapor phase before condensing again on the substrate. CVD is based on precursor molecules reacting or decomposing on the substrate surface producing the desired material film.
The high number of different PVD methods is caused by the different requirements for the deposition of different materials, the possibility to deposit on large areas and the need for edge coverage or a directed deposition. Evaporation refers to methods, where the material to be deposited is evaporated for example by heating it in a resistive heated boat or by an electron beam (with up to $15\,\mathrm{keV}$). The vapor particles then move through the vacuum of the deposition chamber towards the substrate, where they condense. The choice of the specific method depends on the material to be deposited. Due to the high energy density reached electron-beam evaporation can also evaporate tungsten or carbon. Evaporation is however limited concerning the deposition of compounds.
Sputtering refers to processes where material particles are ejected from the surface of a material target due to bombardment with energetic particles. Typically an argon plasma is used. Sputter deposition also allows easy deposition of materials with high melting points and compounds. While in compounds some elements might have a higher sputter rate leading to a changed chemical composition on the surface of the target at the beginning of the process, after some pre-sputtering an equilibrium forms and the material composition of the target is deposited. Sputter processes also allow the addition of reactive gases during sputtering (e.g. oxygen), allowing for example the deposition of oxides or nitrides using a metal target. The different types of sputter deposition (e.g. DC sputtering, RF sputtering, magnetron sputtering, high-power impulse magnetron sputtering) differ in the generation of the plasma used. Compared to evaporation sputter deposition is less directional and thus less suitable for lift-off processes.
Pulsed laser deposition is a PVD method similar to evaporation, where the material is evaporated using a pulsed laser with high intensity ($\approx 10\,\mathrm{MW/cm^2}$) building a plasma on top of the material surface. The method allows the deposition of films with complex stoichiometry.
CVD processes are based on a precursor molecule reacting on the surface and thereby depositing the desired material. This requires a suitable volatile precursor that reacts or decomposes to the desired material. To reduce reactions in the gas phase, that might form particles, the process generally is conducted at low pressure. The reaction energy is provided by high temperatures of typically several $100°\mathrm{C}$. CVD is appropriate for the deposition of films on complex surfaces.

For deposition at lower temperatures plasma-enhanced chemical vapor deposition (PECVD) can be used.
Heating the substrate during deposition can strongly influence the properties of the deposited films, as it provides additional energy leading to higher mobility of the atoms/molecules condensed at the surface.
Depending on the surface energy γ_s of the substrate, the surface energy of the material γ_M and the energy of the interface γ^* different growth modes can occur. If the surface energy of the substrate is larger than the sum of the surface energy of the material and the energy of the interface $\gamma_s > \gamma_M + \gamma^*$, the adsorpt atoms/molecules first build a complete layer, before a new layer is started. This leads to layer-by-layer or "Frank Van der Merwe" growth. In the opposite case $\gamma_s < \gamma_M + \gamma^*$ the adsorpt atoms/molecules build nuclei that grow leading to island or "Volmer-Weber" growth. However, growth can also start with layer-by-layer growth and switch to island-growth after several layers. This is called "Stranski-Krastanov" growth.

2.5.2 the ALD deposition method

In contrast to most other deposition methods ALD provides deposition in discrete steps of single atomic layers (molecular layers - molecular layer deposition) [140, 144]. As in common CVD there are different precursors reacting on the surface of the sample depositing the desired material. However, while in CVD the reaction of the precursors happens constantly, the process is performed in a self-limiting way in ALD. The difference can easily be understood looking on the presence of the different precursors in the deposition chamber and the film growth during the deposition process. In CVD both precursors are constantly present in the chamber at the same time over the whole deposition process. The film grows linearly with time. In ALD the film grows in small steps each representing one individual deposition cycle. In such a cycle the first precursor is present in the chamber for some time so that a layer of precursor molecules can bind to all surfaces. Then the chamber is purged with an inert gas until all unbound molecules of the first precursor are completely removed from the chamber. Then the second precursor is let into the chamber where it can react with the bound molecules of the first precursor (see Figure 2.9).

the ALD cycle

The basis for each ALD deposition process is the individual ALD cycle that is continually repeated until the desired amount of material is deposited. The ALD cycle starts with the first precursor entering the vacuum chamber where it binds to all surfaces. The way the precursor binds to the substrate is essential for the complete process. There are two types of adsorption processes, *physiosorption* arising from weak interactions and the stronger *chemisorption* involving the formation of chemical bonds [146]. As physiosorption is not specific on the molecule-surface pair, the adsorption may occur in multilayers. In contrast in chemisorption only one layer adsorbs to the surface [146], thus resulting in a much more controlled process. So for an ALD process chemisorption of the precursor molecules to the substrate surface is desired. Also the adsorption should run into saturation when the surface

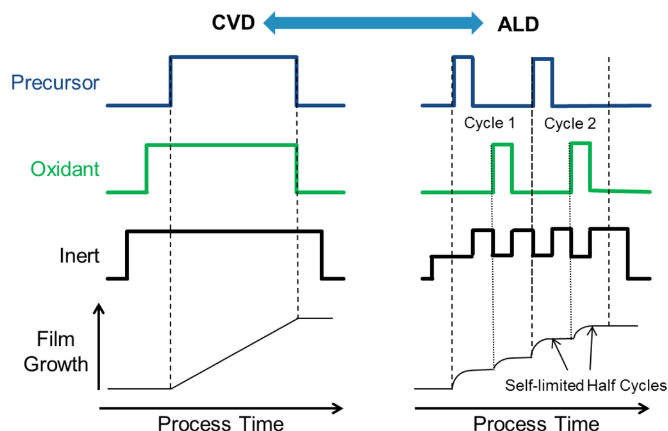


Figure 2.9: Schematic comparing the basic gas flow sequence to the chamber for CVD and ALD. The bottom line shows the expected film growth over time (taken from [145]).

is exposed a long time, and the adsorption should be irreversible. Otherwise there might be desorption during the next step in the ALD cycle [146]. The cycle then proceeds with a pump and purge step removing all the remaining unbound precursor molecules from the gas phase. Then the second half of the cycle begins with the second precursor (e.g. an oxidant) entering the chamber reacting with the molecules of the first precursor forming one single material layer. Another pump and purge step removes all reaction products as well as remaining molecules of the second precursor from the gas phase leaving the chamber as it has been at the beginning of the cycle. Then another ALD cycle might be started (Fig. 2.10).

growth per cycle

For most deposition methods a deposition rate is used to characterize the deposition process run. For electron beam evaporation this deposition rate for example depends on the material and on the acceleration voltage of the electron beam. For ALD the term “deposition rate” can not be used in the same way. Since there is no deposition per unit of time as the word “rate” suggests. ALD is not a continuous deposition process, but the deposition is done in steps. The term “growth per cycle” (GPC) is used to state how much material is deposited in one single cycle. However, a deposition rate can be given for every ALD process, but the term refers to more technical information. As there is some specific GPC the deposition rate gives some information on how long one cycle takes. This strongly depends on the specific process and the reactor construction.
The growth per cycle is a material and process specific value. It cannot be increased in the same way that the deposition rate in other deposition methods can be. The amount of grown material in one cycle depends on the used precursor and the adsorption process.
The amount of material grown in one cycle depends on the amount of precursor chemisorpt in the first half of the cycle. This precursor can for example be a compound reactant of type ML_n, with a central atom (M) and ligands (L). The film grown would then be MZ_x with Z being part of the second precursor. There are three mechanisms how a compound reactant ML_n can

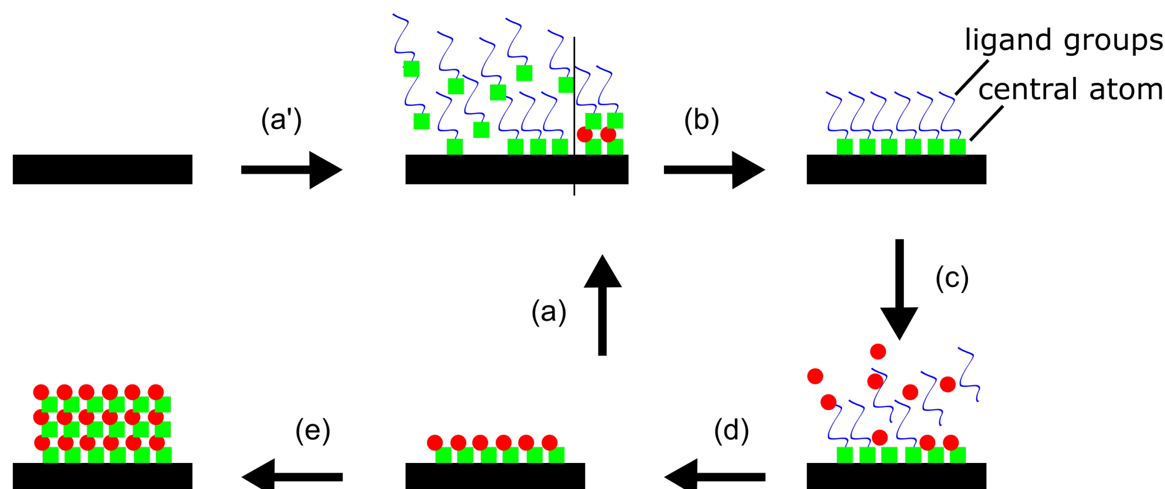


Figure 2.10: Schematic representation of ALD: (a'/a) Start of a new ALD cycle. Precursor 1 – consisting of a central atom and ligand groups – is introduced. (b) The chamber is purged and pumped off. Only those precursor molecules bonded to the surface remain in the chamber. (c) Precursor 2 is introduced and reacts with precursor 1 forming one monolayer of the deposited material. (d) Remaining reaction products and precursor molecules are removed from the chamber. End of the ALD cycle. The steps (a), (b), (c) and (d) are repeated until the target thickness is reached (e).

bind onto a solid surface: *Ligand Exchange*, *Dissociation* and *Association* (Fig. 2.11) [147]. In *Ligand Exchange* the molecule splits and releases one of its ligands as gaseous reaction product. In *Dissociation* the precursor molecule is split too, but there is no release of an reaction product into the gasphase. In *Association* no ligand is split from the molecule.

In the ALD process the surface is exposed to the precursor until saturation is reached. Saturation is typically caused by steric hindrance of ligands or a limited number of bonding sites [147].
Steric Hindrance of Ligands refers to the big size of the precursor molecules. Due to the big ligand groups, covering some amount of the surface, they can prevent other precursor molecules from binding to the surface in this area, although there might be free bonding sites.
Limited Number of Bonding Sites means that there might be not enough bonding sites to cover the hole surface with precursor molecules.
This means that the central atoms M of the precursor molecules in one monolayer chemisorpt precursor ML_n are not very densely packed, and therefore such a monolayer does not convert to one monolayer of the ALD-grown material MZ_x.
So to deposit one monolayer of material using atomic layer deposition one deposition cycle is insufficient. And also the growth per cycle can not be estimated from the density of the material and its molecular size.
As growth mode for ALD layers layer-by-layer (Frank Van der Merwe) growth seems natural, as multilayer adsorption is excluded for ALD. However, as less than a monolayer is deposited per cycle, other growth modes are possible too [146]. The GPC can vary within the first cycles deposited due to diferent substrate-precursor interaction [144]. Island growth is common for ALD processes, when the material deposited differs from the substrate material [144]. Whether the deposited films are armorphous or crystalline depends upon material, temperature and

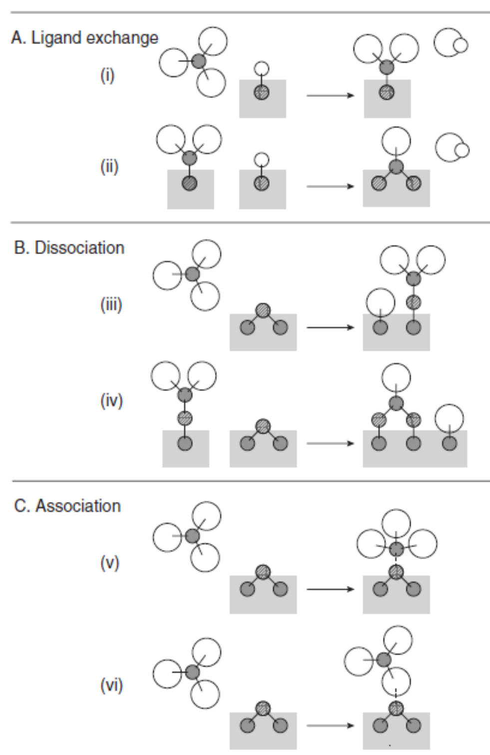


Figure 2.11: Different possible chemisorption mechanisms of precursor molecules ML_n on a surface (taken from [147]). Ligand exchange comes along with the release of a gaseous reaction product (i) and can also occur for precursor molecules already bound to the surface (ii). In the dissociation process the precursor molecule is split, but no product is released (iii). The process can also proceed further on the surface (iv). In the association process the precursor molecule ML_n can form a bond between its central atom M and the surface (v) or between the ligands and the surface (vi).

substrate. While aluminium oxide deposited with ALD is primarily armorphous, zinc oxide grows almost always in a crystalline form; for titanium nitride it depends on the process details whether the film grows amorphous or crystalline and for titanium oxide both has been reported [144]. Using $TiCl_4$ and water as precursors amorphous TiO_2 (T<$165°$C), anatase structure ($165°$C - $350°$C) or rutile structure (>$350°$C) have been reported [148].
In general it can be concluded that films will be crystalline with higher probability for thick films, pure materials and higher temperatures during deposition [144].
With the high dependence on surface chemistry of ALD film growth, it is obvious that the ALD process is influenced by the substrate material and its surface. Therefore, the GPC can change with increasing number of cycles until a saturation value is reached when the surface is covered by a sufficient thick ALD layer and the substrates' surface loses its influence. This effect can for example be observed during ALD deposition on polymers [149].
The directed modification of the surface can be used to achieve area selective ALD film growth [150, 151].

2.5.3 process characteristics

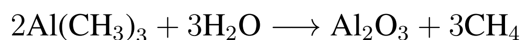
For an ALD process the dependency on the different process parameters is different than in a common CVD process. The main characteristic is the independency of the growth per cycle from the applied amount of precursor within a certain range. Of course GPC is lower, if there was too little amount of precursor, so that not enough precursor molecules were available to cover all binding sites on the substrate. However, if there is enough precursor to cover all binding sites any extra amount of precursor would not affect film growth, as it could not bind to the surface and would therefore be pumped off in the following pump and purge step. The amount of precursor used in the process is controlled via the duration of the precursor pulse. So from the point where the duration of the pulse is long enough to supply enough precursor to cover all binding sites, the GPC does not change for longer pulse duration. This is in strong contrast with conventional CVD deposition, where the amount of precursor determines the growth rate, and can therefore be used to examine an ALD process [152]. This characteristic is also responsible for the perfect conformal deposition on complex three-dimensional surfaces. Deep trenches are not as easily accessed by precursor which for CVD leads to a lower deposition rate at the bottom of deep trenches. For ALD however, it does not matter if the precursor concentration at the bottom of the trench is a 1000 times less then on top of the trench, as long as it is enough to form one layer on the surface, the layer growth will be the same as on top of the trench. This of course only holds, if there is enough time for a sufficient amount of precursor to reach the bottom of the trench [153].
Closely related to the duration of the precursor pulse are the purging steps between the precursor exposure. These steps have to be long enough to safely remove all precursor molecules from the gas phase. This again might take longer for samples with deep trenches. If the purging pulse was too short, remaining precursor molecules can lead to reactions in the gas phase and a continual growth CVD component. As a consequence the GPC can increase, while the layer homogeneity and film quality can decrease as the process is no longer pure ALD.
For the process temperature also a specific range exists for each ALD process where an ALD process takes place and the GPC does not change with temperature [153]. For temperatures outside of this range different effects can lead to an increase or decrease of the GPC, though. For low temperatures the reactivity of the precursor can be too low, preventing complete reactions and thus leading to an decreased GPC. Or the precursor can condense on the surface. In this case purging will not be sufficient to drive out the excess precursor molecules and the GPC will increase. On the other hand for high temperatures the precursor might either decompose, leading to an additional CVD component, and thus an increased GPC, or the precursor molecules can desorb during the purge step leading to a decreased GPC. Of course in none of these four cases does a proper ALD process take place.
So, within a specific range ALD processes do not depend on the exact values of the process parameters and are thus “robust”. Therefore, ALD allows homogeneous deposition over a large area. Also the risk of gas phase reactions is much lower than in conventional CVD processes. The deposited layers are of high quality with low defect density and can be controlled on a fundamental level.

2.5.4 different ALD types

Just as there is "normal" thermal CVD and plasma-enhanced CVD (PECVD) there are also different types of ALD. Different alternative processes have been developed not only to decrease deposition temperature, but to expand the number of materials that can be deposited using ALD [140, 141, 154].

thermal ALD

In thermal ALD the required energy for the reactions taking place is provided through heat. The process temperature depens on the used precursor, but is typically in the range between 150°C and 350°C [141]. A typical thermal ALD process would be the deposition of Al_2O_3 using $Al(CH_3)_3$ [trimethylaluminium (TMA)] and water:



$$2Al(CH_3)_3 + 3H_2O \longrightarrow Al_2O_3 + 3CH_4$$

Water is a common oxidant in thermal ALD and while the reaction above will also function at low temperatures (below 100°C), a temperature chosen too low will result in extremely long cycle times (minutes instead of seconds) as it becomes more difficult to purge the water out of the chamber [154]. On the other hand there are precursors that cannot be used, as they require such high temperatures to react that they would desorb, thus preventing any film growth [154]. ALD is a surface-controlled process and temperature is an important parameter concerning the question if the precursor molecules can bind in an irreversible and self-terminating way to the surface as required for an ALD process to take place [146].

plasma-enhanced ALD

Plasma-enhanced ALD (PEALD) procedures were developed to lower deposition temperature enabling the use of precursors that would otherwise decompose before the intended reaction takes place [140, 141]. There are three plasma-enhanced methods: radical-enhanced ALD, direct plasma ALD and remote plasma ALD. The highly reactive species generated in the plasma can supply high reactivity while only heating up the substrate scarcely [141]. This is because from the different gas species only the electrons are heated significantly in the plasma. Also the plasma exposure only takes place during part of the cycle.

- Radical-enhanced ALD has the plasma generated far away from the zone where the ALD reaction takes place. Due to the long path of the plasma species to the substrate, ions and electrons do not reach the substrate as they recombine on surfaces. The flow of radicals is also reduced, leading to long radical exposure times [141].

- Direct plasma ALD has the plasma generated right on top of the substrate with the substrate stage being the grounded electrode of the plasma generator. The plasma generation close to the substrate leads to a high flux of plasma radicals and ions to the substrate [141].

- Remote plasma ALD has the plasma generator located remotely from the substrate. In contrast to radical-enhanced ALD the electron and ion densities on the substrate are not decreased to zero. In contrast to direct plasma ALD, plasma and substrate conditions can be varied independently [141].

While thermal ALD and plasma-enhanced ALD are the most widely used, also further ALD concepts as laser-assisted atomic layer epitaxy (LALE) have been tried [155, 156].
Puurunen gives an overview on ALD processes based on two reactants [146]. ALD is most suited for the growth of compound materials as oxides and nitrides, but also pure elements have been successfully deposited using ALD.

2.5.5 properties of ALD layers

For the measurement of the electric properties of thin insulating films metal-insulator-metal or metal-insulator-semiconductor samples have to be prepared. The conduction mechanism in such a sample can either be electrode-limited (showing no dependence on layer thickness) or bulk-limited [157].
Al_2O_3 films with > 10 nm thicknesses showed leakage currents of approximately $1\,\frac{\mathrm{nA}}{\mathrm{cm}^2}$ at 2 V [158]. At a voltage of approximately 4.5 V the current rises due to Fowler-Nordheim tunneling [158]. The leakage current depends on layer thickness. For a 12 nm layer dielectric breakdown occurred at $5.2\,\frac{\mathrm{MV}}{\mathrm{cm}}$ [158]. For thick films the dielectric constant was determined as $\varepsilon \approx 7.6$, but decreased with decreasing layer thickness [158].
TiO_2 films come along with high leakage currents of approximately $10\,\frac{\mathrm{nA}}{\mathrm{cm}^2}$ at 0.5 V [159]. The dielectric constant depends on the crystalline structure of the film. For rutile structured TiO_2 a value of 90 respectively 170 depending on the axes is reported [159]. For anatase TiO_2 values between 30 and 40 are reported [159]. For TiO_2 thin films fabricated with other methods, the range of observed values for the relative permittivity includes also values < 6 [160].
The current vs. voltage characteristic of TiO_2 thin films depends on the contact material during measurement, i.e. the metals in a metal-insulator-metal configuration [161]. Depending on the work-function of the metal, the TiO_2/metal contact is not ohmic, but builds a Schottky barrier diode [162].
Further, TiO_2 films have shown resistive switching bahavior [163–165]. Hysteresis in the current vs. voltage diagram was observed for voltage sweeping between -3 V and $+3$ V [163, 164]. For the ratio between the high and low conductive state values > 100 have been observed [163–165].
Resistive switching has been observed for different metal oxides either in a unipolar (switching independent of voltage polarity) or a bipolar (switching depends on the polarity of the voltage) way. While unipolar switching can be explained by the formation or rupture of conducting filaments, bipolar switching is related to electrochemical migration of oxygen ions at the metal/metal oxide interface [166]. The switching of TiO_2 is bipolar and related to oxygen vacancies acting as dopants transferring the insulating TiO_2 into a conductive semiconductor [164, 165]. This was shown by preparation and examination of TiO_x films with intentionally high concentration of oxygen vacancies [164, 165].

Yang et al. explain the switching mechanism of a Pt/TiO_x/TiO_2/Pt structure with changes in the non-ohmic contact Pt/TiO_2 [165]. Depending on the polarity of the applied voltage positively charged vacancies are attracted and drift towards the interface, forming conducting channels. When these channels penetrate the electronic barrier, the device switches to its high conducting state. A voltage with reverse polarity repels the vacancies and the device switches back to its original low conducting state.
Kim et al. explain the switching mechanism of an Al/TiO_x/TiO_2/Al structure with a two-variable resistor model [164]. The oxygen vacancies in the TiO_x act as traps for electrons. The conductivity of the TiO_x is high when the traps are filled and low if they are unfilled. The model divides the TiO_x layer of thickness D into a part $w(t)$ where the traps are filled, and a part $D - w(t)$ where the traps are unfilled. Current flow can then – depending on its direction – either fill up or clear traps and thus change $w(t)$. The total resistance in this model is $R_{\text{total}} = R_{\text{low}}\frac{w(t)}{D} + R_{\text{high}}(1 - \frac{w(t)}{D})$.
The observed resistive switching makes TiO_2 a candidate for the technological realization of a charge-controlled memristor M(q) [167].
As ALD layers provide low defect densities, they are extensively studied as barriers. While $10\,\mu\text{m}$ of polyimide exhibit a water vapor transmission rate (WVTR) of approximately $3.7\,\frac{\text{g}}{\text{m}^2\cdot\text{d}}$ [168] and $10\,\mu\text{m}$ of parylene C exhibit a WVTR of approximately $20\,\frac{\text{g}}{\text{m}^2\cdot\text{d}}$ [169], metal oxide layers deposited using ALD have reached WVTRs below $10^{-4}\,\frac{\text{g}}{\text{m}^2\cdot\text{d}}$ [170]. Low WVTRs have been reported for Al_2O_3 and TiO_2 [142, 171, 172], but commonly Al_2O_3 provides lower WVTRs. Also, the exact deposition process and parameters (e.g. used precursors, thermal ALD/PEALD, deposition temperature) highly influence the achieved WVTR of a coating. For Al_2O_3 films deposited in plasma-enhanced ALD using trimethylaluminum (TMA) and oxygen plasma WVTRs of $4\cdot10^{-3}\,\frac{\text{g}}{\text{m}^2\cdot\text{d}}$ (11.8 nm) and $5\cdot10^{-3}\,\frac{\text{g}}{\text{m}^2\cdot\text{d}}$ (20 nm) in good agreement have been reported from different groups [142, 171]. However, their observances concerning the influence of the deposition temperature on the resulting WVTR are opposing [142, 171].
Klumbies et al. observed exponential decrease in the defect density between 15 nm and 100 nm layer thickness, while the WVTR showed exponential decrease only between 15 nm and 20 nm and sub-exponential decrease above 25 nm [173].
Amorphous Al_2O_3 films have been reported to dissolve in water [143], and thus Al_2O_3 and TiO_2 have been combined to build stable barriers with low WVTRs [174].
In a flexible device the ALD barrier can be compressed or strained, potentially leading to the formation of cracks opening diffusion paths and thus increasing the WVTR of the barrier [92]. Typical critical strain for conventional thin film materials is $0.5\% - 1\%$ [92]. For Al_2O_3 an increase in critical strain with decreasing film thickness has been observed, with a critical strain of $0.88 \pm 0.06\%$ for 125 nm, $1.56 \pm 0.06\%$ for 25 nm and $5.08 \pm 0.08\%$ for 5 nm [175]. An ALD multilayer of Al_2O_3 (10 nm)/TiO_2 (10 nm)/Al_2O_3 (10 nm)/TiO_2 (10 nm) prepared on PES (poly(ether sulfone)) substrate with a thickness of $650\,\mu\text{m}$ withstood 800 bending cycles to a bending radius of 12.5 mm before the WVTR increased [176].
Another application for ALD layers increasing the stability of micro devices, besides their use as water vapor barriers, is through adhesion promotion. For parylene-metal-parylene devices it has been shown that an ALD deposited layer of Al_2O_3 can increase the adhesion between two parylene layers [177].

Chapter 3

Materials and Methods

This chapter comprises all information on the processes used within this work.
The first section describes the concept and overriding idea of the developed process for the fabrication of the system intended to be built. This includes the layout for the demonstrator system based on functionless die-dummies used for the development of the fabrication process. The subsequent sections then describe the individual process components in detail. The second section is on the transfer printing procedure used. It first describes the process for fabricating the stamps and describes all substrates occurring in the process. It then explains how different measurements of the relevant forces appearing during the transfer printing process have been performed. Finally it describes how the transfer printing procedure itself was performed.
The third section explains in detail the embedding procedure developed within this work including a foregoing step for turning the array.
The forth section describes the processes for the fabrication of the conducting tracks on top of the embedded arrays using MEMS fabrication processes. This includes the etching of VIAs (vertical interconnect access) through parylene C and the structuring of the conducting tracks.
The fifth section is on the deposition of layers using atomic layer deposition (ALD) describing all processes used.
The sixth section is on the characterization of ALD layers. It describes the electrical measurements performed, and also the method used to examine the permeation through the ALD layers.

3.1 overall fabrication process

This section first describes the layout of the system that should be fabricated based on the idea of the Neuroflexarray project. Then it describes the overall process developed for the fabrication of this system.
The idea of the project was to build a large microelectrode array with more than 1000 electrodes, covering an area of several mm^2 with the possibility for further scaling up, by embedding an array of tiny CMOS-dies providing multiplexing and thus reducing the number of tracks in the array enabling the fabrication of such a big electrode array. The dies were developed within the project and their size was set to be $250\ \mu m \times 250\ \mu m$. As their spacing within the array would

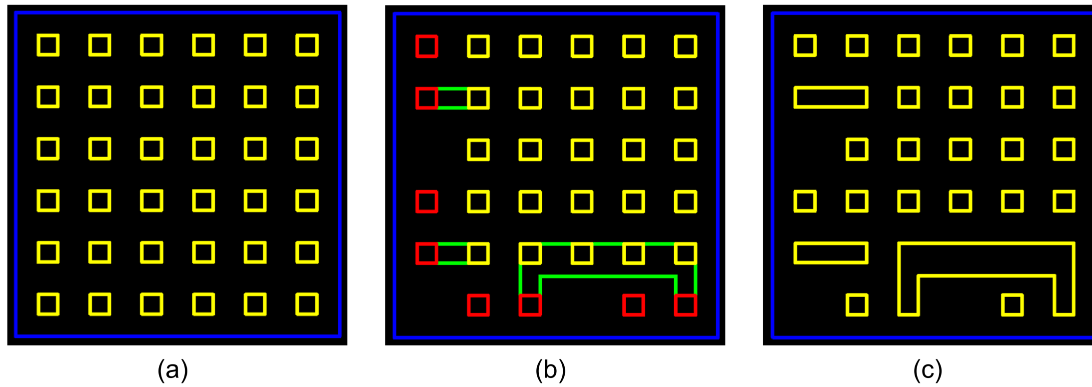


Figure 3.1: Schematic of the layout of the die-dummies. (a) The complete surface area of $250\ \mu m \times 250\ \mu m$ is covered by an 6×6 array of contact pads with a size of $15\ \mu m \times 15\ \mu m$ each and a pitch of $40\ \mu m$. The orientation of the die cannot be seen from the pattern of the contacts. (b) There are 5×5 contacts for the electrodes (yellow) and 11 possible contact sites to contact the die (red). Three of these sites have been removed from the layout, as they cannot be used in order to allow spreading of the conducting tracks to the electrodes. (c) For the demonstrator system some of the contact sites have been merged allowing resistance measurements at the total system.

be about 1 mm, it was decided that they would not have to be flexible by themselves in order to achieve a flexible total system. Their thickness would then be between $100\ \mu m$ and $300\ \mu m$. Each die multiplexes and amplifies the signal of 25 electrodes connected to it thus forming a cluster. It was decided to start with an array size of 7×7 clusters (resp. dies) resulting in an array with $49 \cdot 25 = 1225$ electrodes.

3.1.1 system layout

For the development of the fabrication process a demonstrator system with non-functional die-dummies was drafted, exhibiting the same demands concerning the fabrication process as the system with the functioning dies actually aimed for in the project. The demonstrator system was drafted looking very similar to the original system with the functioning dies.
For the die-dummies metal contact sites were structured on top of a silicon wafer polished on both sides using laser direct writing and a lift-off process. The pattern for one die-dummy was repeated every $300\ \mu m$ giving the die-dummies a size of $250\ \mu m \times 250\ \mu m$ budgeting $50\ \mu m$ for separation between the individual dies. The pattern of the contact sites except for a few modifications was the same as the pattern of the contacts sites on the real dies, based on a 6×6 array of pads of $15\ \mu m \times 15\ \mu m$ size with a pitch of $40\ \mu m$ (Fig. 3.1 (a)). From these 36 possible contact sites 25 are the contacts for the electrodes of the cluster. The remaining eleven sites are available for the six tracks that have to contact the die from outside the system: positive voltage (V_{DD}), negative voltage (V_{SS}), Clock (CLK), Reset (Res), Reference (Ref) and Data. From these eleven contact sites the one in the corner and the two in the middle of the sides are impractical and should not be used in order to allow a symmetrical spreading of the electrodes from the contact pads (Fig. 3.1 (b)). For the demonstrator system some of the contact sites were merged

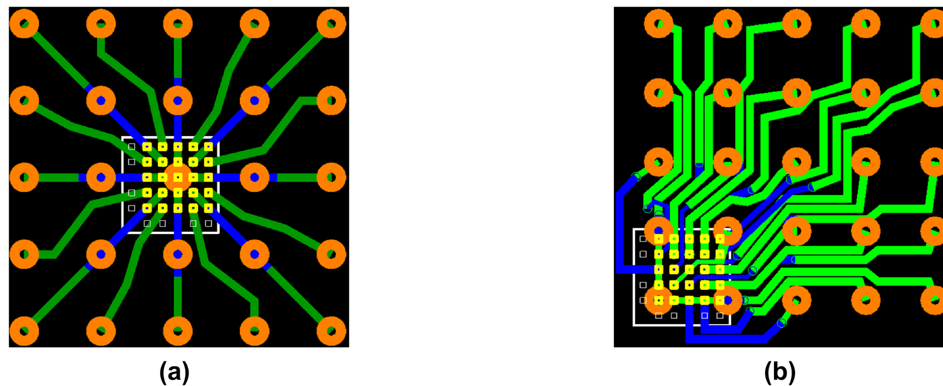


Figure 3.2: Sketch of a die and the conducting tracks (blue = lower layer, green = upper layer) spreading off the electrodes (orange) from the contacts on the die (yellow). (a) Design based on a symmetric star-like spreading with the die in the center. (b) Asymmetric design for spreading with the die in the lower left corner of the electrode array.

in order to allow resistance measurements on the completed system (Fig. 3.1 (c)). On the front side two contact pads were connected by merging them with four other contact pads forming a "contact-bridge". Otherwise there would be no possibility to check weather the die-dummies have been contacted properly, as the system is completely passive. The die-dummies were realized with the contact sites made of aluminum and chromium with a thickness of ≈ 400 nm. These die-dummies were used for the development of all sub-processes.
Besides the dies both demonstrator and functioning system consist of the conducting tracks connecting the dies with the electrodes and the outer electronic system and thus forming the electrode array. As each die forming a cluster builds up a little electrode array by itself the way the electrodes are spread out from the dies is a central point in the layout of the conducting tracks of the total system.
Two possibilities for the spreading of the electrodes from the dies have therefore been considered. The first possibility would be to place the central electrode of the 5×5 array above its contact site on the die spreading the electrodes in a symmetrical way in all directions like the points of a star. This layout idea leads to a balanced distribution of the conducting tracks on top of the die (Fig. 3.2 (a)). However, on two sides the tracks for the spreading have to pass the contact sites for the connection of the die to the rest of the system. This leads to the above mentioned – and considered – restriction that three locations for contact sites cannot be used.
The second possibility would be to place the lower left electrode of the 5×5 array above its contact site on the die (Fig. 3.2 (a)). This leads to higher track densities on top of the die, as all tracks must follow the same two directions (up or right). The advantage is that no tracks have to pass the contact pads for connecting the die to the rest of the system. Both possibilities require two layers of conducting tracks.
The highest number of conducting tracks per area within the system is reached on top of the dies during the spreading of the electrodes. So in order to allow as high a track spacing as possible the first possibility – coming along with a more homogeneous distribution of the conducting

tracks on top of the dies – was chosen both for the demonstrator and the original system with the real dies. The lower layer of conducting tracks was not at one level with the dies contact sites as there was a passivation on top of the dies that was just opened above the contact sites to be contacted. The upper layer of conducting tracks was also the layer of the electrodes, these were just openings in the passivation covering the upper layer of conducting tracks. The tracks for the inner nine electrodes were directly routed in the upper conducting layer, while the tracks for the outer sixteen electrodes were routed in the lower layer, until they reached the other electrodes and then were routed in the upper conducting layer. So the spreading of the electrodes from one die (forming a cluster) required all available space in the lower conducting layer within a square spanned by two electrode distances d as well as all available space in the upper conducting tracks within a square spanned by four electrode distances d on top of each die. For a cluster interval ℓ this resulted in $\ell - 2 \cdot d$ of free space in the lower layer of conducting tracks and $\ell - 4 \cdot d$ of free space in the upper layer of conducting tracks between the clusters where the tracks connecting the dies from outside the array could be routed. For a homogeneous electrode distribution $\ell = 5 \cdot d$ and thus the available free space to route the tracks is $3 \cdot d$ in the lower and d in the upper layer.
As the transfer printing only allows multiples of the initial spacing the cluster spacing in the demonstrator system was chosen to be $900\,\mu\text{m} = 3 \cdot 300\,\mu\text{m}$. The size of the array was set to 7×7 die-dummies with columns A to G and rows 1 to 7. The die-dummies were all connected to 25 electrodes each that were homogeneously distributed leading to an electrode spacing of $\frac{900\,\mu\text{m}}{5} = 180\,\mu\text{m}$. The electrode diameter was set to $30\,\mu\text{m}$ except for the one in the lower left corner of each cluster that had a diameter of $50\,\mu\text{m}$. The tracks for the spreading of the electrodes from the die-dummy were drafted with a width of $20\,\mu\text{m}$. Minimal spacing between tracks within the same layer was always > $5\,\mu\text{m}$. Each die-dummy was connected to five tracks leaving the array, which is one less than in the system with the real dies. However, while in the system with the functioning dies only one track (Data) has to be guided separate for each die, in the demonstrator system two tracks were guided separate for each die and thus the track density was higher and thus not less challenging as in the system with the real dies. This aberration was done to contact the merged contacts on the die-dummies on both sides separately for each die-dummy in the array. The width of the tracks was $30\,\mu\text{m}$. All the tracks that were guided separately from each die-dummy left the array on the left side, the other tracks that were merged from the different die-dummies left the array on top and on bottom of the array. No tracks were leaving the array on the right side. Around the array were 28 big contact sites allowing easy contact for several exemplary resistance measurements. The following features in the layout could be contacted by the contact sites for measurement:

- "contact-bridge" for the die-dummies: A1, B2, C3, D4, F4, D5, E5, B6, F6 and G7
- "daisy-chain" in different length in the first, sixth and seventh row
- the enlarged $50\,\mu\text{m}$ diameter electrodes of all clusters are together connected to one big reference electrode with a $250\,\mu\text{m}$ diameter outside the array
- 9 normal electrodes of different clusters are connected to contacts sites via their die-dummy

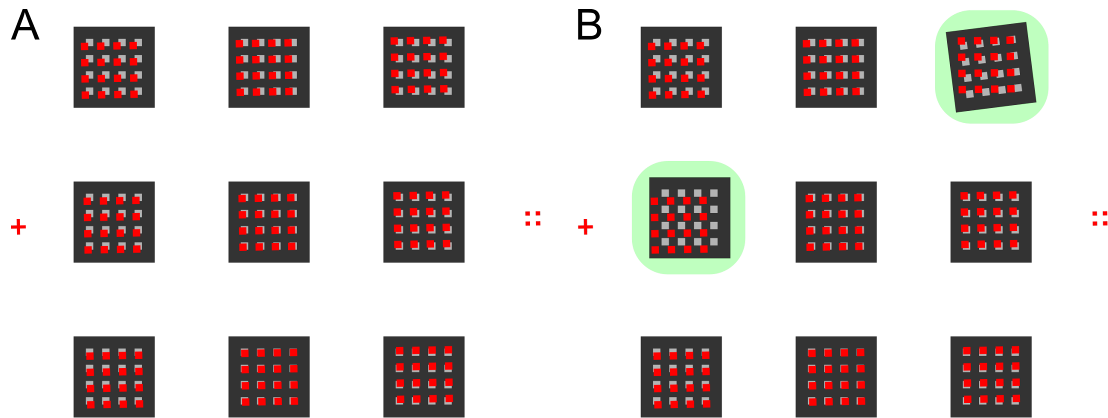


Figure 3.3: Sketch of a photomask being aligned on a 3 × 3 array. A: The relative positiones of the nine dies fit exact, perfect alignment is possible. B: Two of the nine dies are displaced from their ideal position or tilted, respectively. Thus, alignment cannot fit.

3.1.2 fabrication procedure

The connection of the dies to the remaining system was done by directly fabricating the conducting tracks on top of the die array. Metal is deposited using sputter deposition and structured using photolithography and dry etch. This requires the alignment of photomasks on the dies of the array. A satisfactory alignment result can only be achieved when the relative positions of the individual dies of the array to each other are very accurate (Fig. 3.3). In order to enable electrical contact an overlap between the contacts of the dies and the structures on the photomask must be realized. This then gives the maximum displacement for a die from its ideal position in order to preserve the chance of sufficient alignment, it is half the contact pitch on top of the dies and thus $20\ \mu m$.
To achieve such a high assembly accuracy it was decided to choose a fabrication process conserving the wafer die order. As a consequence the spacing of the dies in the array was limited to any integer multiple of the die-spacing on the wafer. Transfer printing as a parallel deterministic assembly procedure was selected as most suitable process and adapted to the specific needs of the dedicated fabrication process.
The use of photolithographic processes for structuring metal and insulating layers to fabricate conducting tracks and VIAs (vertical interconnects between different layers of conducting tracks) requires a planar surface with only a few micrometers of topography, as the photoresists spin coated within these processes are only a few micrometers thick. To achieve a planar surface the array was poured in PDMS. The conducting tracks were fabricated from Ti/Au/Ti, parylene C was used as an insulating layer between different layers of the conducting tracks.
The individual processes for transfer printing, embedding and the fabrication of the electrical connections are described in detail in the following three sections.

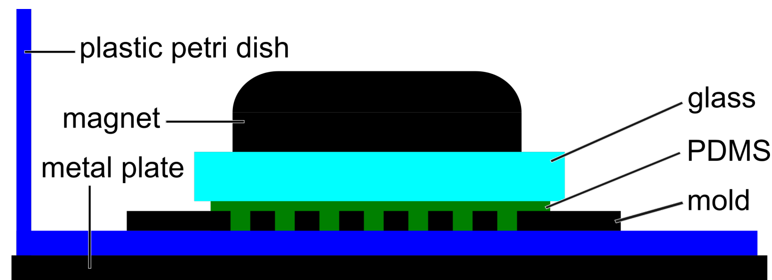


Figure 3.4: Schematic of the stamp casting process using a steel foil mold in a plastic petri dish.

3.2 transfer and assembly of dies

3.2.1 stamp fabrication

The PDMS stamps were casted from the two component PDMS Sylgard 184[1]. Besides the recommended standard mixing ratio of 10:1 (base : curing agent) also a mixing ratio of 20:1 (base : curing agent) was used resulting in the cured PDMS becoming softer. Mixing was performed at 2000 rpm for 2 minutes using a Speed Mixer[2]. For a mixing ratio of 10:1 the Young's modulus is – depending on curing temperature – between 1.32 and 2.97 MPa [79]. Measurements conducted according to *DIN EN ISO 527-1* with samples according to *DIN EN ISO 527-2 Type 1A* confirmed this value for our PDMS. For a mixing ratio of 20:1 the Young's modulus was measured to be about $0.32\,\mathrm{MPa}$. The molds for the casting process were made of steel foil with a thickness of $100\,\mu\mathrm{m}$ or $150\,\mu\mathrm{m}$, respectively. The features of the stamp were cut out using a laser[3]. After cutting the molds were derusted in 10% phosphoric acid for 2 minutes. For the casting the molds were cleaned with isopropanol and then placed in a plastic petri dish. A droplet of PDMS was then placed on top of the structures of the mold. Just enough PDMS was applied to fill all the holes in the mold. Careful application also secured that the PDMS filled all holes without trapping any air. Nonetheless the mold was then placed in a desiccator for 20 minutes. Then a piece of glass (approx. $20\,\mathrm{mm} \times 20\,\mathrm{mm} \times 1\,\mathrm{mm}$) activated in air plasma was placed on top of the mold. By first bringing one edge of the glass in contact to the mold, and then carefully deepening the glass trapping of air bubbles was prevented. The glass builds the backbone of the stamp, with the PDMS just being a thin layer on top forming the stamps profile. Using a metal plate underneath the petri dish and a magnet on top of the glass the stack was pressed together during curing (Fig. 3.4) which was performed at room temperature for two days in order to prevent any shrinkage of the PDMS [78].

3.2.2 donor and receiver substrate

The donor substrate – providing the dies for the transfer printing process – and the receiver substrate – on which the dies are placed in the transfer printing process – are essential for a

[1]Dow Corning, Midland, USA
[2]SpeedMixer DAC 150.1 FVZ-K, Flack Tek Inc., Landrum, USA
[3]ProtoLaser U, LPKF Laser & Electronics AG, Garbsen, Germany

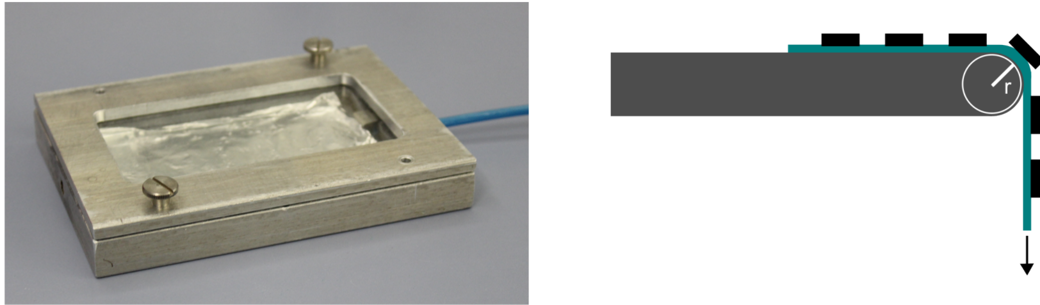


Figure 3.5: Left: Picture of the chamber used to flush the samples with nitrogen during UV exposure. Right: Schematic of how the dies were loosened after exposure, by pulling the sample over an edge with a curvature radius r.

reliably functioning process.
The donor substrate is the substrate the dies are sitting on during and after separation and thus a special dicing tape was chosen that was UV curable. The receiver substrate has to be "sticky" to facilitate reliable transfer of the dies to it. Regarding the following process steps substrates with a thin sugar coating were chosen as receiver substrates. The embedding process starts with another transfer process for flipping the array (see section 3.3.1). There the sugar functions as water-soluble sacrificial layer.

donor substrates

The UV-Tape Adwill D-841[4] was chosen as dicing tape and as donor substrate for the first transfer process. Its high adhesion before UV exposure of 1 N/mm allowed the separation of silicon wafers into individual dies of $250\,\mu\text{m} \times 250\,\mu\text{m}$ size using wafer dicing. The dicing was performed on a DAD 321[5] using two different blades. A wide blade (Z09-SD3000-Y1-60 54× 0.18 A3× 40[5]) resulted in precise cuts with a width of $200\,\mu\text{m}$. A second slender blade (NBC-ZH 2060-SE27 HFDD[5]) resulted in cuts with a width of $\approx 60\,\mu\text{m}$. Dicing was performed under constant water flow with 30,000 rpm of the blade and a feeding rate of 5 mm/s. The tape was only negligibly expandable and therefore suitable in conserving the relative positions of the dies as given on the wafer. After UV exposure the tape exhibited only an adhesion of about 2 mN/mm enabling easy removal of dies.
For exposure a mercury-vapor lamp with an power output of about $40\,\frac{\text{mW}}{\text{cm}^2}$ was used. The tape was then exposed for 13 minutes under nitrogen flow in an aluminum chamber with UV transparent window at the top (Fig. 3.5 left). After exposure the dies were loosened by pulling the tape in a $90°$ angle over an edge with a radius of curvature of $r \approx 0.75$ mm in both dicing directions (Fig. 3.5 right). Afterwards the tape sample was fixed to a rigid handle substrate using double-sided adhesive tape.

[4]Lintec, Japan
[5]DISCO Corporation, Japan

receiver substrates

Pieces of silicon wafer (23 mm × 23 mm) were used as substrates and coated using a solution of sucrose[6] dissolved in deionized water in a 50%-weight ratio. The coating was done using spin coating with 2,500 rpm for 90 s and a drying step in the oven at 100°C for 5 min. The resulting sugar coating was a few micrometers thick and sticky under normal room conditions at air (20°C and about 40% relative humidity).

3.2.3 measurement of pull-off strength

All relevant forces appearing during the transfer process were examined in separate experiments using a tensile testing machine of type Z020[7]. Peel-tests with the UV-tape were performed to see if the exposure was sufficient. The required pull-off strength to pull off silicon pieces from the exposed UV-tape was measured as was the pull-off strength of different PDMS stamps under various conditions.
The peel-tests were performed in accordance to *DIN EN 1939:2003-12* method 1 following the information given in the data sheet of Adwill D-841. Six stripes with a width of 24 mm and a length of 30 cm were cut with a scalpel and carefully attached to the surface of a polished silicon wafer. The surface had been thoroughly cleaned with acetone and isopropanol using a lint-free cloth. After the tape had been attached it was pressed on by twice rolling over it with a 2 kg weighted roll. Three samples were then exposed to UV light for 13 min under nitrogen flow. The wafer was then glued to an aluminum block that could be clamped in the tensile testing machine. The peeling was performed under an angle of 180° with a speed of 300 mm/min over a length of 90 to 95 mm.

required pull-off strength

To measure the force required to pull off silicon pieces from the exposed UV-tape two samples were prepared each allowing six individual measurements. Each sample comprised six 1 cm × 1 cm pieces of double-side polished silicon wafer attached to the UV-tape. The UV-tape was exposed for 13 min under nitrogen flow. One sample was mechanically stressed – simulating a loosening of the pieces – before both samples were glued to the mount of the tensile testing machine. A screw nut was glued to each of the 12 individual pieces, allowing easy connection to the machine (Fig. 3.6 A). The pieces were then pulled off with a speed of 0.6 mm/min, while the force was tracked.

pull-off strength stamps

The pull-off strength of the stamps was measured for different stamp designs. Stamps were prepared from the PDMS mixed in the standard 10:1 mixing ratio and from softer PDMS made with a 20:1 mixing ratio. Three different designs concerning the stamps profile have been fabricated:

[6]Südzucker AG, Germany
[7]Zwick Roell AG, Germany

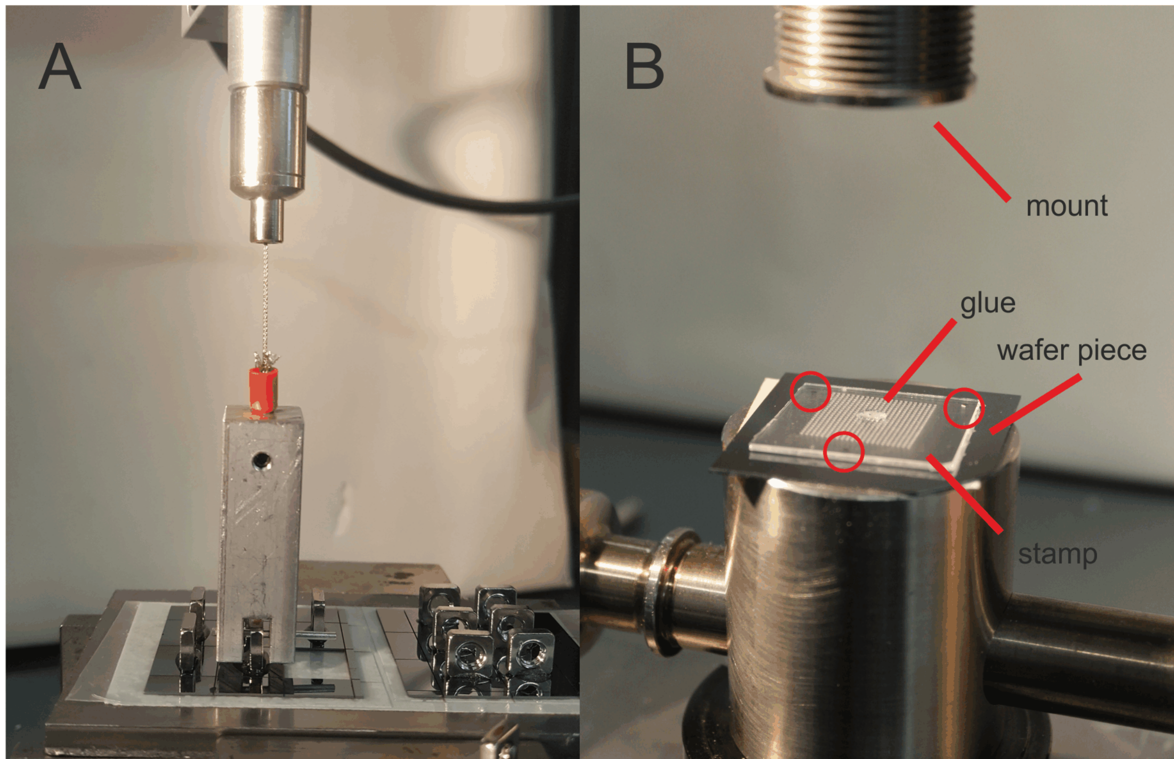


Figure 3.6: A: Picture of the measurement of the required pull-off strength, showing how the individual pieces were connected to the testing machine. B: Picture of the measurement of the stamps pull-off strength. The stamp is placed on three spacers (red circles) above the wafer piece before it is glued to the mount of the testing machine in this position.

- **squares**: 22×22 array of small square bumps with an edge length of $300\ \mu\text{m}$ each
- **circles**: 22×22 array of small circular bumps with a diameter of $350\ \mu\text{m}$ each
- **big squares**: 5×8 array of big square bumps with an edge length of $1\ \text{mm}$ each

with the size of the arrays chosen to achieve an active stamping area of at least $40\ \text{mm}^2$. Assuming pull-off strengths of about $0.025\ \text{MPa}$ – based on literature values [127] – this would results in measurement values of about $1\ \text{N}$ being good measurable. These six different kind of stamps have each been fabricated three times. For the measurements a wafer piece with a polished silicon surface was glued to the tensile testing machine and thoroughly cleaned of any dust. To make sure that during the measurements all bumps of the stamps come to contact with the silicon surface at once the stamps were placed on three silicon spacers ($250\ \mu\text{m}$ thick) on top of the silicon surface. The stamps were then glued to the mount of the testing machine in this plane parallel position and the spacers removed (Fig. 3.6 B). All measurements then followed the following scheme, while the force was constantly measured:

- The stamp is moved down, and the force starts to increase from zero when the stamp first comes to contact with the silicon surface and the bumps of the stamp are compressed.

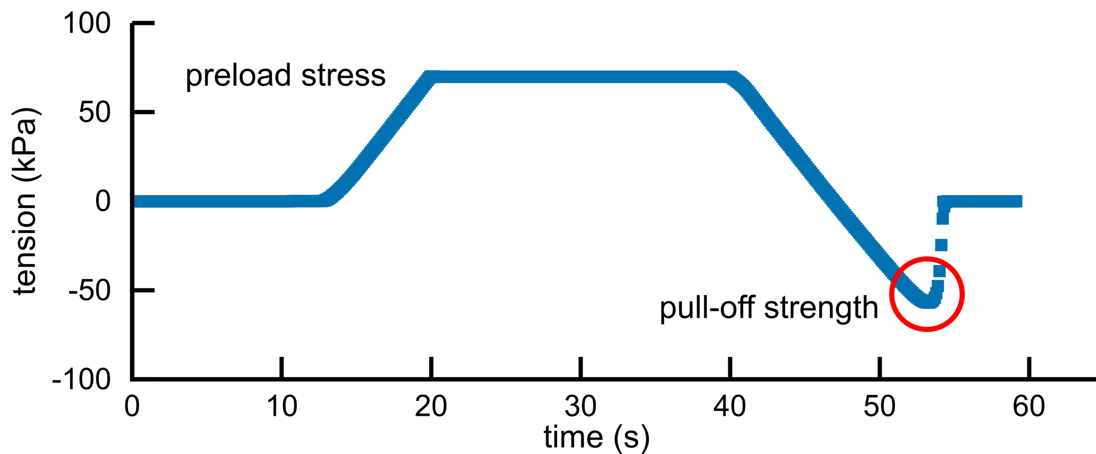


Figure 3.7: Example of the received measurement curves used to extract the pull-off strength of the stamps.

- When a certain preload stress is reached the position is held for 20 s, so that the PDMS of the stamp can adapt to the silicon surface.
- Then the stamp is moved up again and the force decreases. Most tests have been performed with a separation speed of $0.6\,\mathrm{mm/min}$. However, also additional tests with separation speeds between $0.3\,\mathrm{mm/min}$ and $10\,\mathrm{mm/min}$ have been performed.
- After the stamp has passed the position where it first came to contact with the silicon surface the measured force becomes negative and the stamp starts pulling on the surface until it finally detaches from the surface and the force goes back to zero again.

The absolute value of the minimum force measured right before the stamp detaches is then taken as the maximum force the stamp is capable to pull with on the silicon surface (Fig. 3.7).

3.2.4 transfer printing

For the transfer printing of the die-dummies (approx. $250\,\mu\mathrm{m} \times 250\,\mu\mathrm{m}$ in size) different stamps were prepared. At the end stamps made from the standard PDMS with a profile depth of $100\,\mu\mathrm{m}$ established as a standard. Concerning the profile different layouts were considered. Bumps with a slightly larger area than the die-dummies would result in contact with the complete die-dummies' area even for small miss-alignment. However, due to the small gap between the die-dummies prior to the transfer printing this could endanger high selectivity. Thus, at the end stamps with $225\,\mu\mathrm{m} \times 225\,\mu\mathrm{m}$ square bumps were used.
For the transfer procedure a Fineplacer Lambda[8] was used (Fig. 3.8). This machine allows the manual alignment and placement of two samples on each other. Therefor one sample is picked up from its horizontal position on a little heatable plate using a vacuum tool on an arm that is then moved to a second upright position. A beam splitter is used to overlay the picture of

[8]Finetech GmbH & Co.KG, Germany

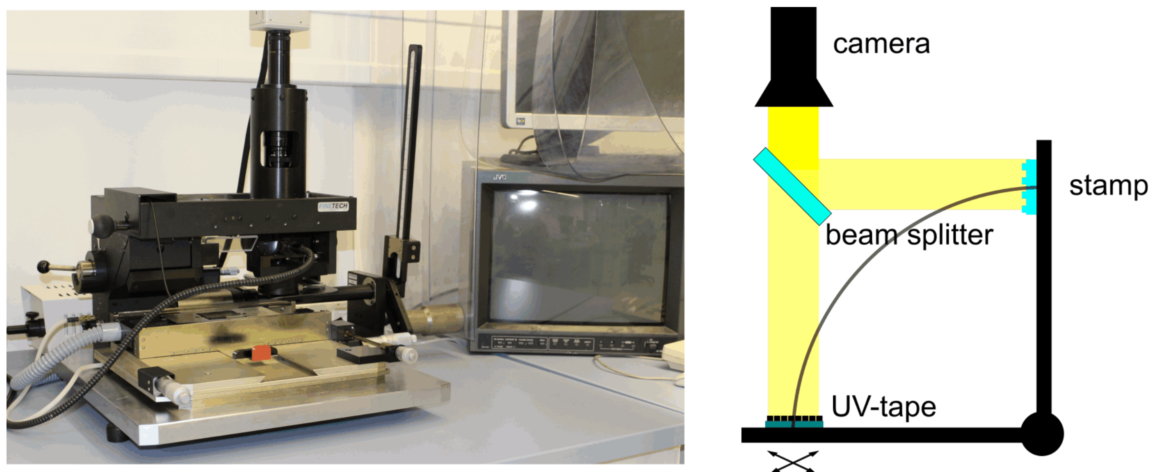


Figure 3.8: Left: Picture of the fineplacer used for the transfer printing. Right: Schematic of the fineplacer showing, how the device allows the alignment of the stamp on the die array. The stamp is mounted on a swinging arm held in upright position. A beam splitter superimposes the picture of the stamp with the picture of the position where the stamp is moved when the swinging arm is moved to its horizontal position. The UV-tape with the dies is placed in this position, where it can be moved precisely to obtain good alignment between stamp and dies.

the sample in the new upright position with its former horizontal position on the plate where now the second sample can be placed. The alignment can then be done by moving the second sample until the superimposed pictures of both samples show good alignment. Then the arm with the first sample is moved down to its original position above the plate placing it exactly on the second sample. A movable weight on the arm allows adjustment of the contact pressure. However, as the arm moves down in an arc, contact normally is not perfectly perpendicular. The plate itself can be moved vertically. For taking off the dies from the prepared UV-tape sample the PDMS stamp was attached to the vacuum tool of the movable arm, while the UV-tape sample was placed on the plate. The tape sample is then moved until the stamps profile is well aligned on the separated dies. The stamp was then brought to contact with the dies for 30 seconds before it was detached and moved to the upright position. The UV-tape sample was then replaced by one of the sugar coated substrates. The stamp was moved down to contact, before the plate was heated up to 120°C in order to dry the sugar coatings surface. Temperature and contact were held for 5 minutes. The stamp was then inspected and potentially adhering dies were removed. The stamp was then flushed with deionized water to be sure that no sugar adheres to the PDMS of the stamp. After drying with nitrogen the stamp was reused for the next transfer.

3.3 embedding of dies

3.3.1 flipping of the array

At the beginning of the developed embedding process the array – attached to a sugar coated substrate after the transfer printing process (sec. 3.2.2) – was flipped by transferring it to another

substrate (Fig. 3.9 (a) to (b)). The receiving substrate in this transfer was a shellac coated substrate. The shellac softens for temperatures above 80°C and is soluble in ethanol, but not in water.
A 50%-weight and a 35%-weight solution of shellac[9] in ethanol were prepared and coated on glass substrates (49 mm × 49 mm × 1 mm) using spin coating. Different spin speeds and durations were used to obtain layer thicknesses in the range of approximately 1 μm to 35 μm. After spin coating the shellac film was cured on a hotplate at 120°C for 5 minutes. A square with the approximate size of the die array was engraved on the backside of the glass substrate. For the transfer the sugar coated substrate was attached to the vacuum tool of the movable arm of the fineplacer (Fig. 3.8), while the shellac coated substrate was placed on the table. A rough alignment was done, securing the placement of the array inside the engraved square of the shellac coated substrate with only little tilt. For the transfer the shellac film then was softened or made “sticky”, before the two substrates were brought to contact. When the shellac was hard again, both substrates were stuck together. The sample was then placed in a petri dish as deionized water was poured on top. This dissolved the sugar within 20 to 30 seconds releasing the former sugar coated substrate, leaving the array transferred into the shellac.

3.3.2 pouring in PDMS

A first layer of 3 μm of parylene C was then deposited onto the sample with the array sitting upside down (Fig. 3.9 (c)). To increase the adhesion of the parylene C to the dies the following pretreatment was applied:

- 5 min Ar-plasma at 250 W
- 5 min O_2-plasma at 250 W
- 5 min adhesion promoter A 174 ((3-Methacryloxypropyl)trimethoxysilane)[10] from gas-phase

During parylene deposition the edges of the substrate were masked using Kapton tape[11]. After the parylene deposition, taking place at room temperature, the Kapton tape was removed. The parylene then only covered the center of the sample, while at the edge of the sample an about 2 mm wide frame stayed uncovered. The sample was then placed on a hot plate and heated to 120°C in order to soften the thermoplastic shellac. Little spacers made from silicon wafer (1.5 mm × 1.5 mm) were then by hand placed in the corners of the sample where the shellac was not covered by the parylene. They were pressed into the softened shellac. When removed from the hotplate the sample cooled down and the shellac solidified with spacers stuck to the substrate. Next the surface of the samples was activated with 90 s of air plasma, before a primer[12] was spin coated (15 s at 1000 rpm) onto the surface. The samples then rested in a closed box with increased relative humidity for about 90 minutes, so that the primer had time

[9] Schellack Astra, Dictum GmbH, Germany
[10] AB 109006, abcr GmbH, Karlsruhe, Germany
[11] 4118 Silicone 1 MIL Kapton Polyimide Tape, Intertape Polymer Group, USA
[12] 1200 OS Primer, Dow Corning, USA

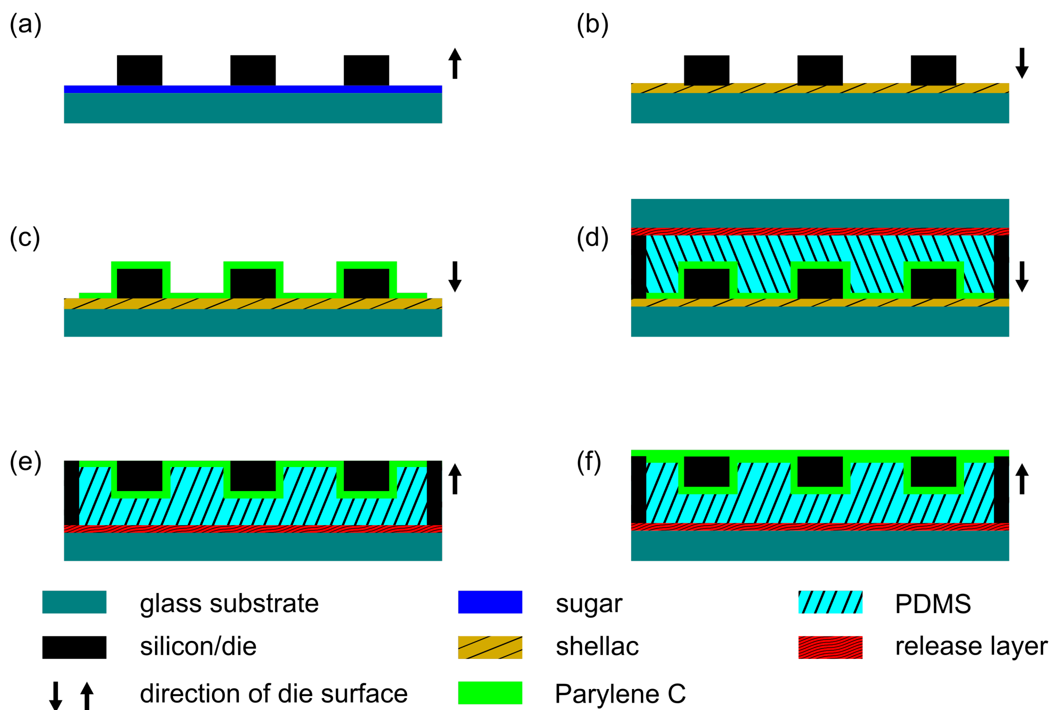


Figure 3.9: Schematic of the embedding process: (a) Die array on sugar coated substrate. (b) The array is transferred to a shellac coated substrate, turning it upside down. (c) Deposition of 3 μm of parylene C. (d) Spacers are placed in the corners of the substrate. PDMS is poured on the sample before placing a second substrate on top. (e) After the PDMS is cured the first substrate is removed using the shellac as release layer. (f) Another layer of 3 μm parylene C is deposited on the planar surface.

to react with the moisture. New glass substrates were prepared by completely masking their backsides with Kapton tape. Four samples were always placed in one quadratic petri dish of $15\,\text{cm} \times 15\,\text{cm}$ size. The two component silicone rubber Sylgard 184[13] was then mixed in the recommended 10:1 mixing ratio and poured onto the samples. The samples were then placed in a desiccator for at least 20 minutes to remove trapped air bubbles. In the next step the prepared glass substrates were carefully placed on top of the samples. By first placing one edge on the sample and then slowly overturning until it laid up on the spacers of the sample no new bubbles were trapped. A sufficient amount of PDMS assured the expulsion of PDMS under the glass substrate during this process step, further decreasing the risk of trapping air bubbles. When the glass was in good overlap with the sample, magnets were used to press this stack together. The PDMS then cured at room temperature for two days (Fig. 3.9 (d)).
When the PDMS was cured the samples were removed from the petri dish and all surplus PDMS was cut away with a scalpel. Removal of the Kapton masking released a clean PDMS free surface of the upper glass substrate. The samples were then turned upside down and placed on a hot plate at 120°C softening the shellac. Careful pressure applied from the side could then

[13]Dow Corning, USA

lift off the old former shellac coated substrate (Fig. 3.9 (e)). To wash the shellac away the samples were then placed in an ultrasonic bath in ethanol for 3 minutes. The samples were then dried using nitrogen. With a scalpel all excess PDMS was cut off the sample. Another 3 μm of parylene C were then deposited onto the samples using the same pre-treatment as before (Fig. 3.9 (f)).

3.4 fabrication of electrical connections

The fabrication of the foil-system on top of the die array including the two layers of conducting tracks required two processes. One for etching VIAs through the parylene C used as insulating material. And another process for fabricating conducting tracks.

3.4.1 fabrication of VIAs

Three layers of VIAs need to be fabricated. The first is for opening the parylene passivation on top of the dies' contact sites, the second is for connecting the first and second layer of conducting tracks and the third one is to open the top parylene coating to the upper layer of conducting tracks at the electrodes.
The fabrication process for the first VIA layer includes the first lithographic step on top of the embedded die array and thus the process includes the alignment of a photomask on the die array. Three different processes are conceivable for the fabrication of the VIAs (Fig. 3.10). A process based on a bright-field mask, meaning the mask was transparent except for the areas where VIAs were intended to be fabricated, was favored.
The parylene was etched using reactive ion etching (RIE) with oxygen at a pressure of 200 mTorr and a power of 200 W.
For masking three different processes have been tried: etching against negative resist (Fig. 3.10 (a)), etching against a hardmask (Fig. 3.10 (b)) and etching against positive resist (Fig. 3.10 (c)). The last process requires a dark-field mask and is thus only suitable for the second and third layer of VIAs, when there are marks for the alignment. However, the flank angles in the process with the positive tone resist are more favorable, than in the process with the negative resist and hence the process results in VIAs with sloped side walls.
negative resist mask
The negative tone resist AZ 15 nXT[14] was spin coated, exposed and developed using the following recipe:

- application of 2.5 ml AZ 15 nXT
- 5 s spin coating with 300 rpm
  15 s spin coating with 2500 rpm
- softbake for 100 s at 90°C and 180 s at 110°C on a hotplate

[14] MicroChemicals GmbH, Germany

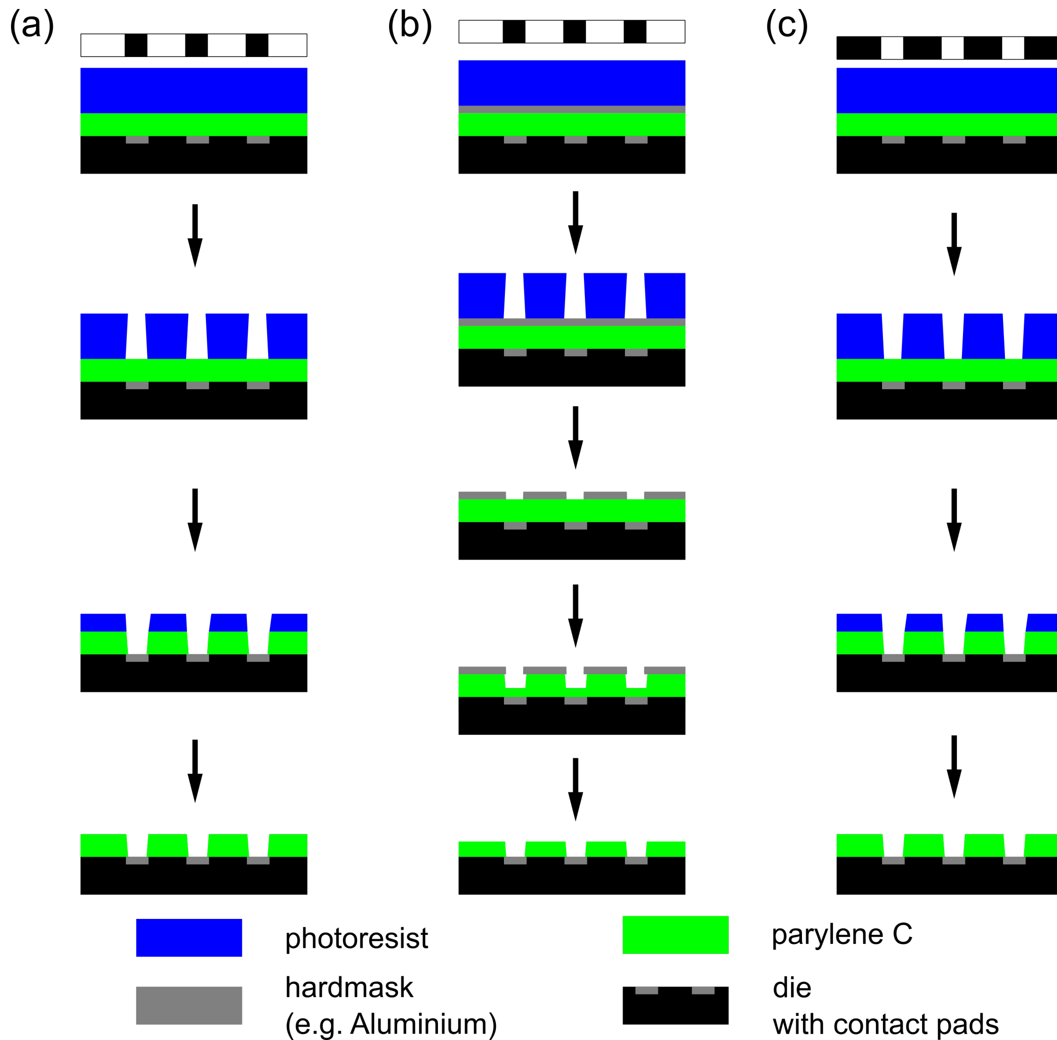


Figure 3.10: Schematics of three different processes for the fabrication of the VIAs. The processes (a) and (b) are based on a bright-field masks allowing the alignment of the mask on the array without alignment marks. The process (c) is based on a dark-field mask. (a) A negative tone resist is structured using photolithography. The VIAs are then dry etched against the structured resist mask. (b) A metal is deposited onto the surface. Then a negative tone resist is structured on top, according to (a). The resist mask is then used to wet etch the metal layer, serving as hardmask during VIA etching after the resist is removed. The VIAs are only partially etched in a first step. Once the hardmask is removed using wet etch, the parylene is dry etched until the VIAs are opened. (c) A positive tone resist is structured and the VIAs etched against this resist mask.

- exposure in soft-contact mode with a dose of 400 mJ/cm^2 (i-line filter) using a MA6[15] mask aligner
- post-exposure bake for 1 min at 120°C on a hotplate
- development in AZ 826 MIF[14] for about 90 s and rinsing in deionized water

The resist was always given enough time to cool down to room temperature between the

[15] SÜSS MicroTec, Germany

different process steps. The parylene was then etched until the VIA was completely formed, before the resist mask was dissolved in a DMSO (dimethyl sulfoxide) bath at $\approx 70°C$.
hardmask
As material for the hardmask aluminum and chromium have been used. About 200 nm of the hardmask's material were deposited on the samples using sputter deposition. Then the negative resist AZ 15 nXT was processed on top following the same recipe as described above. The hardmask was then wet etched against the resist before the resist was dissolved. Chromium was etched using TechniEtch Cr01[14]. For structuring the hardmask an etching time of approximately 3 minutes was required, removing the hardmask took approximately six minutes. Aluminum was etched using TechniEtch Al80[14]. To improve wetting and enable the structuring of the hardmask, 2 minutes of air plasma were applied prior to the etching which took approximately 12 minutes. Removing the hardmask at the end took approximately four minutes.
After structuring the hardmask the resist was dissolved in DMSO (dimethyl sulfoxide) at $60°C$ for 1 h. Afterwards the parylene was etched. After the etching of the VIAs the hardmask was removed in another wet etching step using the same etching solutions. As the VIAs of the first VIA layer go down to the aluminum contacts of the dies for this step the parylene is not etched completely, the hardmask is then removed, before a second dry etch step is performed to completely open the VIA. Otherwise the etching solution attacks – meaning etches – the contacts of the dies while the hardmask is removed.
positive resist mask
The usage of a positive tone resist requires the use of a dark-field mask, and thus no alignment of the mask on the array is possible. Hence, a process for the fabrication based on a positive tone resist is only feasible for the fabrication of the second and third layer of VIAs, when there are already alignment marks. The positive tone resist AZ ECI 3027[14] (also used for the structuring of the conducting tracks) was once applied as mask for etching VIAs.

3.4.2 fabrication of conducting tracks

The conducting tracks were fabricated following established processes. Ti/Au/Ti was sputter deposited onto the samples and etched against a resist mask that had been prepared using the positive resist AZ ECI 3027[14]. The resist mask was prepared using the following recipe:

- application of 2 ml AZ ECI 3027
- 5 s spin coating with 1000 rpm
  20 s spin coating with 2000 rpm
- softbake for 2 min at $90°C$ on a hotplate
- exposure in soft-contact mode with doses between $450\,mJ/cm^2$ and $900\,mJ/cm^2$ using a MA6[15] mask aligner
- post-exposure bake for 90 s at $110°C$ on a hotplate
- development in a $1:5$ mixture of AZ 351B[14] and deionized water for about 40 s, rinsing in deionized water

- hardbake for 30 min at 120°C in an oven

The resist was always given enough time to cool down to room temperature between the different process steps.

3.5 deposition of ALD layers

Within this work ALD layers have been deposited using two different machines. The *MyPlas*[16] has a radio-frequency generator and generates a capacitively-coupled plasma in direct plasma configuration. The machine is in principle also capable of thermal ALD, but this was never used during this work. The recipes for the different processes have been developed observing the growth per cycle (GPC) while varying precursor pulse duration, plasma duration and purging times. If the GPC showed the typical invariance against deviations of these parameters the process was assumed to be ALD. The second machine used was the "*Oxford*"[17] which could be used for thermal ALD or in remote-plasma configuration using an inductively-coupled plasma. On both machines different processes have been used to deposit different materials.

3.5.1 TMA + O_2

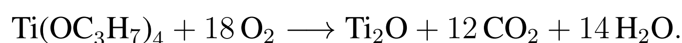
For the deposition of Al_2O_3 trimethylaluminium [$Al(CH_3)_3$] (TMA) has been used as precursor. Only plasma-enhanced processes have been used:

$$2\,Al(CH_3)_3 + 4\,O_2 \longrightarrow Al_2O_3 + 2\,CO_2 + 4\,CH_4 + H_2O.$$

In the *MyPlas* the process was used in direct-plasma configuration at a temperature of 100°C and a plasma power of 150 W. The resulting GPC was approximately 0.16 nm. In the *Oxford* machine the process was run using remote plasma at a temperature of 120°C and a plasma power of 300 W. The resulting GPC was approximately 0.15 nm.

3.5.2 TTIP + O_2

To deposit TiO_2 both for thermal as well as for plasma-enhanced processes titanium tetra-isopropoxide [$Ti(OCH(CH_3)_2)_4$] (TTIP) was used as precursor. Compared to processes using $TiCl_4$ as a precursor the growth per cycle is only about one third [178]. Also the temperature of the deposition process is limited to temperatures below 350°C due to decomposition of TTIP [178].
In the plasma-enhanced ALD process with oxygen as the second precursor the reaction is [152]:



$$Ti(OC_3H_7)_4 + 18\,O_2 \longrightarrow Ti_2O + 12\,CO_2 + 14\,H_2O.$$

In the *MyPlas* the process was used in direct-plasma configuration at an temperature of 100°C and a plasma power of 150 W. The resulting GPC was approximately 0.052 nm. Using the

[16] Plasma Electronic GmbH, Neuenburg am Rhein, Germany
[17] Oxford Instruments, Abingdon, England

Table 3.1: Summary of the different ALD processes used to deposit TiO_2.

machine	plasma	plasma power	temperature	precursor 1	precursor 2	GPC (nm)
MyPlas	direct plasma	150	100	TTIP	O_2	0.052
Oxford	remote plasma	300	120	TTIP	O_2	0.040
Oxford	remote plasma	300	300	TTIP	O_2	0.046
Oxford	-	-	300	TTIP	H_2O	0.032

remote-plasma configuration of the *Oxford* machine processes at 120°C and at 300°C have been conducted, both using a plasma power of 300 W. The GPC for the process at 120°C was approximately 0.040 nm, while the process at 300°C resulted in a GPC of approximately 0.046 nm.

3.5.3 TTIP + H_2O

Depending on the temperature, different decomposition products of the TTIP are possible [179]. As the reaction products have not been analyzed no reaction equation can be given for the process. Thermal ALD using TTIP and water was only run at the *Oxford* machine at a temperature of 300°C, exhibiting a GPC of approximately 0.032 nm.

The different ALD processes used to deposit TiO_2 are summarized in Table 3.1. For all monolayers deposited, the layer thickness was determined using a NanoCalc-XR reflectometry system[18]. The resolution of this system is 0.1 nm, but the GPC is calculated by dividing the layer thickness by the number of cycles used for its deposition. However, good measurement of the layer thickness required the deposition of layers with a thickness of at least 10 nm which required more than 100 deposition cycles. The given GPCs with three decimal places are thus the result of averaging over more than 100 cycles. For multilayers the film thickness was not measured, but calculated based on the GPCs of the monolayer processes.

3.6 characterization of ALD layers

3.6.1 electrical characterization of ALD layers

To measure the electrical properties of the ALD layers grids of gold stripes with measurement fields at their crossings were prepared as samples (Fig. 3.11 left). As substrates 22.3 mm × 22.3 mm pieces of silicon wafer, with a 1 μm SiO_2 surface for good electrical insulation, were used. For reasons of easy fabrication and to prevent the formation of protruding edges and tips at the border of the measurement fields they were fabricated using evaporation and a shadow mask.
The masks were made from 100 μm steel foil cut with a laser (like the molds for the fabrication of the PDMS-stamps described above). For the vertical stripes 5 nm of titanium were evaporated

[18]Ocean Optics Germany GmbH, Germany

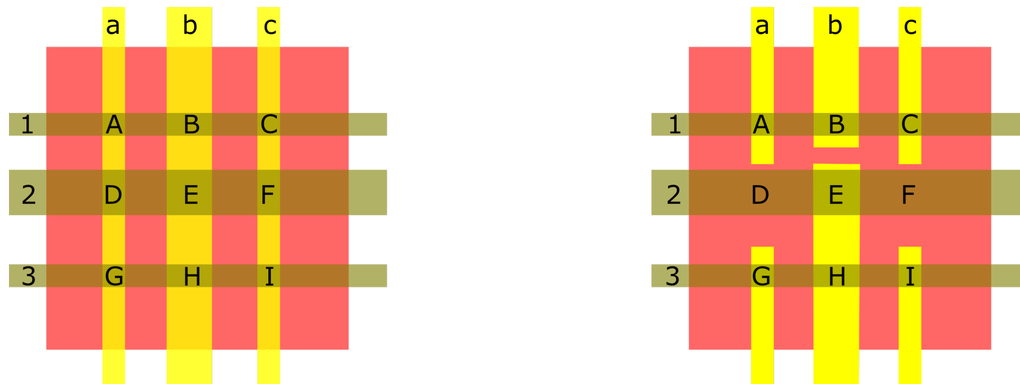


Figure 3.11: Drawing of the used samples for electrical measurements. Three vertical gold stripes were evaporated on top of a silicon wafer with a 1 µm SiO_2 surface using a shadow mask. The ALD layer was then deposited on top of these stripes before evaporating three horizontal stripes on top using a shadow mask again. In a first design this resulted in nine measurement fields (left). Later the vertical stripes were interrupted leaving only seven measurement fields (right).

for adhesion promotion before evaporating approximately 100 nm of gold. The samples were then cleaned in acetone and isopropanol and the ends of the stripes masked during ALD layer deposition using Kapton tape[19]. For the top stripes only about 23 nm of gold were evaporated using a shadow mask. So the ALD layer was never exposed to any chemicals or etched in any way, leaving only the risk of scratches during preparation of the samples.

The stripes had different width of 1 mm and 2 mm resulting in measurement fields of different area on their crossing points (1 mm^2, 2 mm^2, 4 mm^2). As the stripes could be contacted on both ends, a simple resistance measurement using a multimeter could be used to check if the sample was properly contacted prior to measurement.

The sample layout was later enhanced with slight modifications. With the vertical stripes interrupted (Fig. 3.11 right) the number of measurement fields per sample decreased to seven and no control of proper contact to the stripes was possible. However, this new design erased parallel current paths through other measurement fields than the one intended to be measured. With the horizontal stripes named *1*, *2* and *3* (top to bottom), the vertical stripes named *a*, *b* and *c* (left to right) and the nine measurement fields named *A*, *B*, ..., *I* (from top left to bottom right) one would for example have to contact *a* and *1* in order to measure field *A* (see Fig. 3.11). However, in order to flow from *a* to *1* current could also take four parallel paths besides the direct one through *A*. Those parallel paths would pass the fields: *DEB*, *GIC*, *GHB*, *DFC*. For the contacting to measure field *B*, *b1* there would be the parallel paths through the fields: *AGH*, *HIC*, *ADE*, *CFE*. For the contacting to measure field *E*, *b2* there would be the parallel paths through the fields: *DAB*, *DGH*, *BCF*, *HFI*. For all remaining fields due to symmetry it is clear that there are also four parallel paths passing three other fields.

Assuming each field acts as a capacitor, an equivalent circuit can easily be drawn. As the layer is the same for all fields, the capacity of each field is the specific capacitance of the layer times the area of the field. Thus, a correction factor to calculate the specific capacitance from the

[19] 4118 Silicone 1 MIL Kapton Polyimide Tape, Intertape Polymer Group, USA

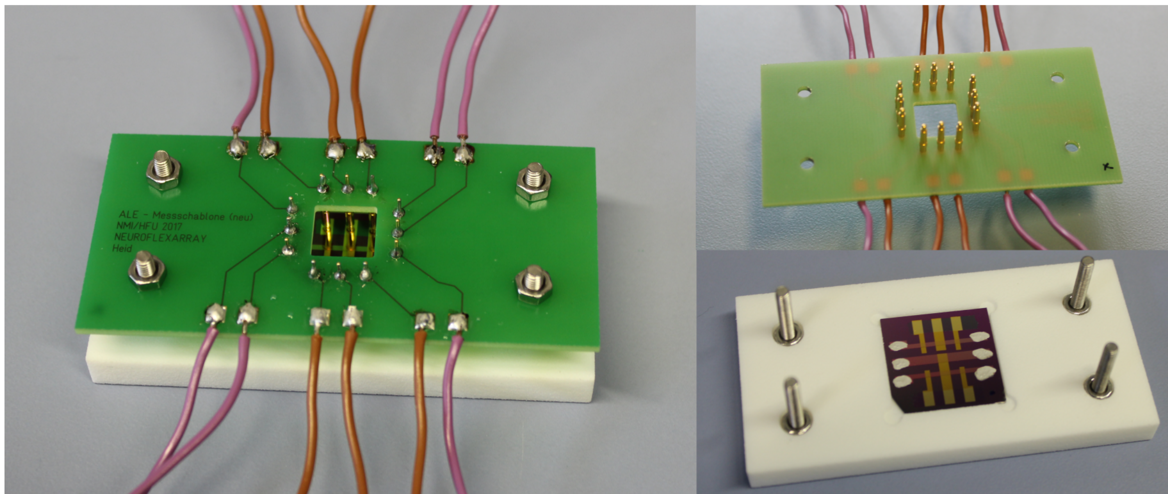


Figure 3.12: Pictures from the used self-built setup for contacting the samples. Upper right: Printed circuit board with spring contact probes. Lower right: Laser sintered plastic part holding a sample. Left: Setup as during measurement.

measured value can be calculated. However, if the resistance of the layer is finite and the fields cannot be modeled by a single capacitance, but a resistance in parallel has to be taken in account, the model is more complicated. Also the current passes different fields in different directions and therefore asymmetrical behavior of the layers cannot be seen.
To contact the samples during measurement a printed circuit board with spring contact probes was built (see Fig. 3.12). The contacts of the upper gold layer were reinforced with conductive adhesive to prevent the contact probes from damaging the thin gold metalization.

AC measurements

The impedance measurements were done using an impedance gain-phase analyzer[20]. The measurements were performed using an amplitude of 100 mV in the frequency range between 1 Hz and 1 MHz. It was also possible to apply an additional DC voltage during measurement. The result of each measurement was plotted in a Bode plot and a model consisting of a resistor R_1 in series with the resistor R_2 and the capacitance C_1 that are in parallel was fitted to the data (Fig. 3.13 left). While R_1 represents the line resistance of the sample in the measurement setup R_2 represents the resistance of the layer being examined and C_1 the capacitance of the plate capacitor like composition of the examined insulating layer between the two gold contacts.

DC measurements

All DC measurements were performed using a source measure unit[21]. In all measurements performed the current flowing through the sample was measured with a defined voltage applied. However, different protocols have been used.

[20]Solartron SI 1260, Solartron Metrology, GB
[21]Keithley 236, Keithley Instruments, USA

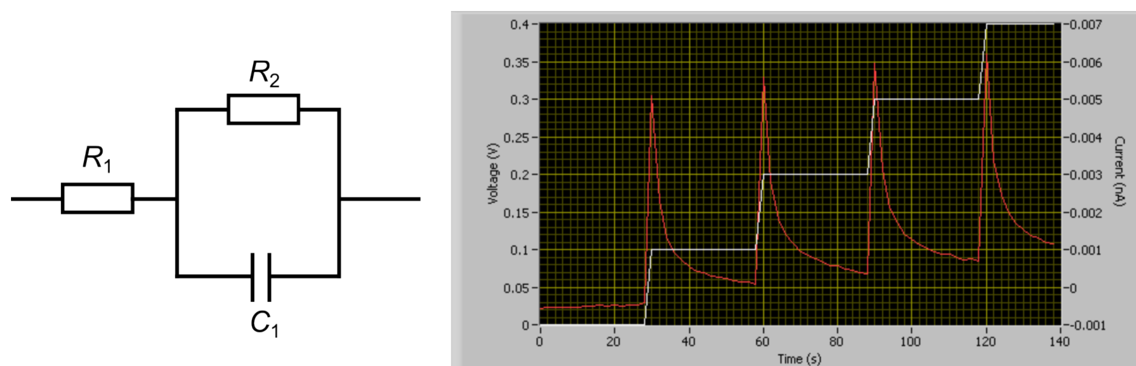


Figure 3.13: Left: The equivalent circuit that was fitted to the measured impedance spectra. Right: Picture showing how the leakage current measurements were performed. Voltage was increased in steps every 30 seconds (white line). After each voltage step the current (red line) was high but decreased fast with time. As value for the leakage current for the applied voltage the current value immediately before the next voltage step was taken.

Current was measured over time after individual voltage steps to examine the charging behavior of the plate capacitor formed by the sample and to check for unexpected nonlinear behavior.
To determine a leakage current through the sample the voltage was increased in steps and the current just measured after waiting for several seconds in order to allow charging currents to decay (Fig. 3.13 right).
Finally the dielectric strength of the layers was determined by increasing the voltage until electrical breakdown occured. Appearance of electrical breakdown could either be recognized in the current-voltage diagram or directly observed through the appearance of light flashes coming along with failure.

3.6.2 permeation measurements

The permeation through ALD coated foil samples was examined using a helium based method providing the helium leakage rate in units of mbar $\cdot\, \ell/\mathrm{s}$ and the barrier improvement factor (BIF) which is the ratio of the leak rate through the uncoated and the coated foil.
Measurement with helium instead of water vapor provides the advantages of low background and fast diffusion. For the precise measurement of samples with low permeation rates the background of the gas used for the measurement has to be low. This is easy to accomplish for helium which has a partial pressure in air of only 5.2 ppm. In contrast water appears in vast amounts. A low water vapor background would therefore require extreme dry atmosphere and the heating of all surfaces to get rid of any adsorbed water molecules. Further due to its small molecule size helium diffuses faster than water and thus reduces the measurement time.

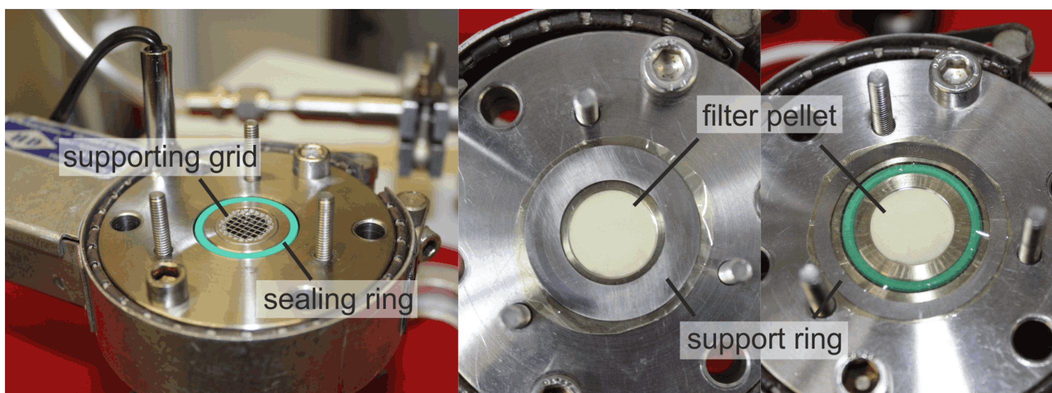


Figure 3.14: Pictures of the part of the measurement setup where the sample is placed. The sample is trapped between the sealing ring and an identical sealing ring pressed to the sample from top. Left: Grid with 1 mm lattice spacing as supporting structure. Middle and right: Filter pellet as supporting structure and foil sample placed on the measurement area. For the sample in the middle picture the ring glued to the sample covers the foil where the sealing ring is pressed against the foil. The sample in the right picture has a larger ring glued to it, so that the ring is completely outside the measurement area.

samples

The samples for measurement had to be foils with a diameter of at least 25 mm. Different foils were used for measurements:

- 125 µm thick Kapton foil[22]
- 6 µm thick polyimid foil, prepared by spin coating PI2611[23], curing was performed at 350°C
- self-deposited parylene C foils

The 125 µm thick Kapton foil was mechanically stable and did not roll up due to internal stress of the deposited ALD layers. The samples based on the thinner self-prepared foils were prepared while still attached to a glass substrate. When all layers were deposited a ring made of 100 µm thick steel foil was glued[24] to the sample preventing the foil from rolling up and simplifying handling (Fig. 3.14). The foil was then cut around the ring, before it was detached from the glass substrate by storing it in deionized water at 60°C until the foil detached.
During measurement the samples face strong mechanical load due to a pressure difference between the two sides of the foil pressing the foil against a support structure. Thus, aim of the sample preparation was a foil where the ALD coating faces as little stress as possible. Therefore, also parylene/ALD/parylene stacks have been prepared as foils, aiming for the ALD layer sitting in (or close to) the neutral axis and thus preventing elongation or compression during deformation (bending) of the foil.

[22]Kapton 500 HN, Hauler & Hermann GmbH, Filderstadt, Germany
[23]DuPont, Wilmington, DE, USA
[24]Trans 7 Clear, MAC GmbH, Austria

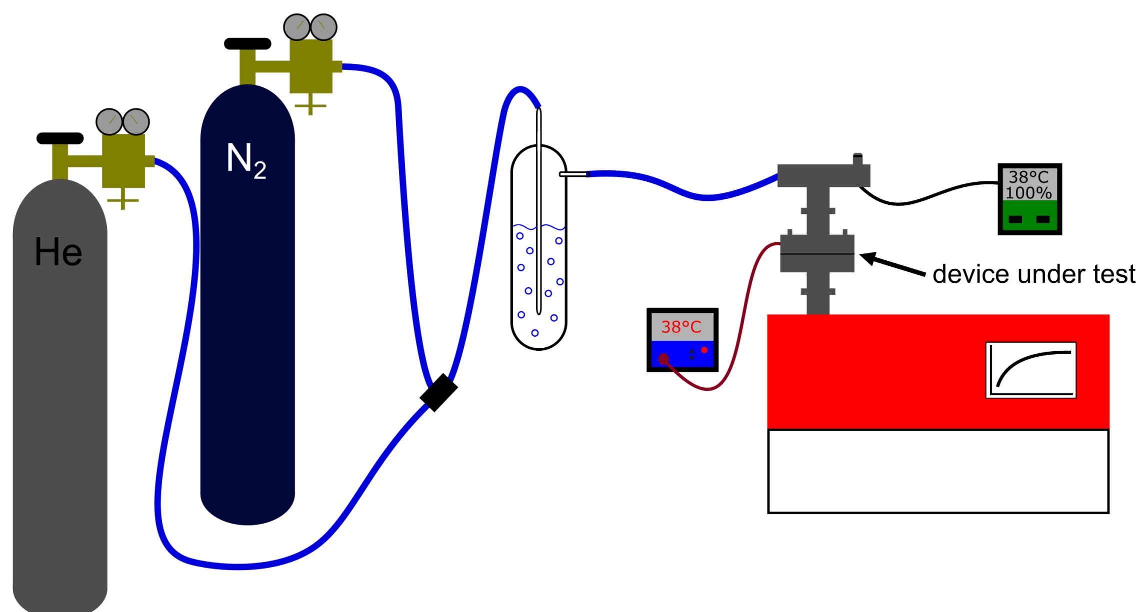


Figure 3.15: Schematic of the gas permeation measurement setup based on a helium leak detector. The foil-sample is placed right on top of the detector. While at the lower side of the sample there is vacuum, there is constant helium flow at atmospheric pressure on the upper side of the sample. The helium is guided through a water filled bubbler. Nitrogen can be used to flush the setup between measurements.

setup

The setup used for the measurements was based on a helium leak detector ASM 340[25] (sketch shown in Fig. 3.15). The sample was placed between two tubes and divided the setup into two halfs. The half underneath the sample was connected to the helium leak detector. The half above the sample allowed to pass by gas on the sample. In order to induce more realistic body like conditions the gases were guided through a water filled bubbler before reaching the sample leading to high relative humidity and the tube the sample was placed on was heated to $\approx 38°C$. The measurement area was circular and had a diameter of 22 mm. During measurement helium was flushed through the setup and the leak detector evacuated the lower half of the setup leading to a pressure difference of 1 bar between both sides of the sample. To mechanically support the sample in the middle of the measurement field where the tube opening with 1.5 cm in diameter is, different structures as a grid or a filter disc[26] could be placed in this opening (Fig. 3.14). Between the individual measurements the setup could be purged with nitrogen.
When helium was flushed through the setup the helium leak rate measured by the leak detector slowly increased before reaching saturation. This saturation value was then taken as leak rate through the sample. Each sample was measured three times. Between these three measurements the setup was vented and the sample anew placed on the measurement field.

[25]Pfeiffer Vacuum GmbH, Aßlar, Germany
[26]VitraPOR Spezial-Filterplatte Por. 4, ROBU Glasfilter-Geraete GmbH, Germany

Chapter 4

Results

The following chapter comprises the presentation of the results achieved that are then discussed in the next chapter. The chapter is divided into separate sections for the different parts of the developed fabrication process: transfer and assembly, embedding and the fabrication of electrical connections. The fourth section describes the mechanical properties of the developed foil-system, and the fifth section presents the results concerning the characterization of ALD layers.
The first three sections on the different steps of the developed overall fabrication process are arranged in chronological order as they appear during the fabrication of the envisioned device and describe the same samples in different steps during their manufacture.
The final section then presents the results from the fabrication of the complete demonstrator system by combining all these processes.

4.1 transfer and assembly of dies

This section first presents the results of measurements of the pull-off strength required to pull off silicon pieces from the exposed UV-tape and the maximum pull-off strength of the fabricated PDMS-stamps. Then it presents the results from the actual transfer printing process providing the samples for the following fabrication steps described in the next two sections.

4.1.1 measurement of pull-off strengths

The unexposed UV-tape peeled off in a sharp $180°$ angle as it was supposed to in accordance with the measurement procedure. A mean adhesion of 0.91 ± 0.01 N/mm was measured. The exposed tape stripes peeled off in a wide bow and the measured adhesion was only 0.16 ± 0.08 mN/mm.

required pull-off strength

For the sample that had not been mechanically stressed the pieces were pulled off perpendicularly leading to a sharp drop of the force in the force-elongation diagram. The mean measured

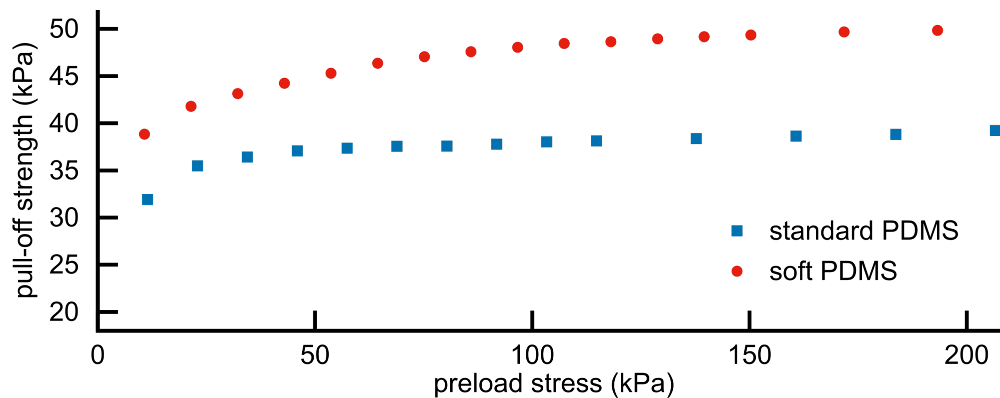


Figure 4.1: Dependence of the pull-off strength on the preload stress for stamps made of standard respectively soft PDMS.

force was 6.14 ± 0.70 N corresponding to a strain of 61 ± 7 kPa. For the sample, where the pieces had been loosened by applying mechanical load to the exposed tape, the pieces peeled off slowly starting from one side, resulting in non-perpendicular pull off with a mean measured force of 1.65 ± 1.15 N. There was much higher variation of the values, and the minimum pull-off force measured was only 0.52 N.

pull-off strength stamps

Measurements with different **preload stresses** between 10 kPa and 210 kPa have been performed for stamps made of the standard and the soft PDMS. For the stamps made of the standard PDMS in the range between 50 kPa and 200 kPa no influence of the preload stress on the pull-off strength could be observed (Fig. 4.1). For the stamps made of the soft PDMS there was only slight dependence of pull-off strength for preload stresses above 75 kPa (Fig. 4.1). Therefore all following measurements were done using a preload stress of approximately 100 kPa.
A dependence of the stamps pull-off strength on **PDMS hardness** and **stamp design** was examined measuring each stamp fabricated three times using a separation speed of 0.6 mm/min (Fig. 4.2).
For the stamps made of the standard PDMS mean values of 27 ± 5 kPa (square bumps with 300 µm edge length), 23 ± 4 kPa (circular bumps with 350 µm diameter) and 26 ± 6 kPa (square bumps with 1 mm edge length) were obtained.
For the stamps made of the soft PDMS mean values of 32 ± 5 kPa (square bumps with 300 µm edge length), 44 ± 1 kPa (circular bumps with 350 µm diameter) and 54 ± 10 kPa (square bumps with 1 mm edge length) were obtained. The mean values and standard deviations are all based on nine separate measurements.
The difference in pull-off strength between the stamps made of the standard and the soft PDMS was significant with a p-value $< 0.1\%$ (t-test). The differences between the different stamp designs were not significant for the stamps made of the standard PDMS (p-values above 25%, t-test). For the stamps made of the soft PDMS the difference between the stamps with the small square bumps and the big square bumps was significant with a p-value $< 0.1\%$ (t-test).

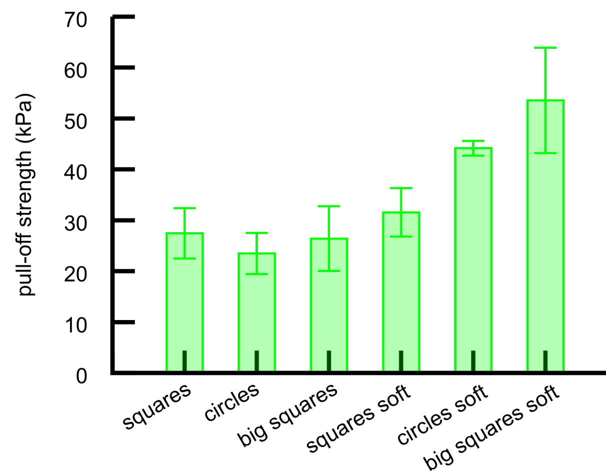


Figure 4.2: Mean pull-off strength and standard deviation for the different stamp designs. Each stamp design was measured using three different stamps thrice each. The separation speed was $0.6\,\mathrm{mm/min}$.

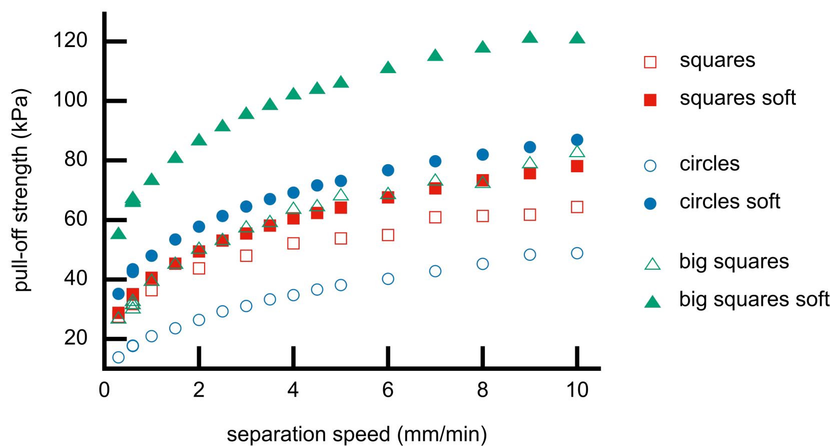


Figure 4.3: Measured pull-off strength for different stamps at different separation speed. For all stamps the pull-off strength increases with increasing separation speed.

For all stamps made of the standard PDMS the obtained values from two stamps differed by less than 5%, while the measured pull-off strength of the third stamp was notable lower. For the stamps made of the soft PMDS, the design with the small square bumps also resulted in two good agreeing values and one differing significantly, while the values obtained for the stamps with the circular bumps all differed by less than 5%. The measured pull-off strength of the three stamps with the big square bumps made of the soft PDMS differed by more than 20%.
The values from the three measurements performed sequentially with each stamp slightly decreased in almost every case. The decrease from measurement to measurement was in the range of 5%.

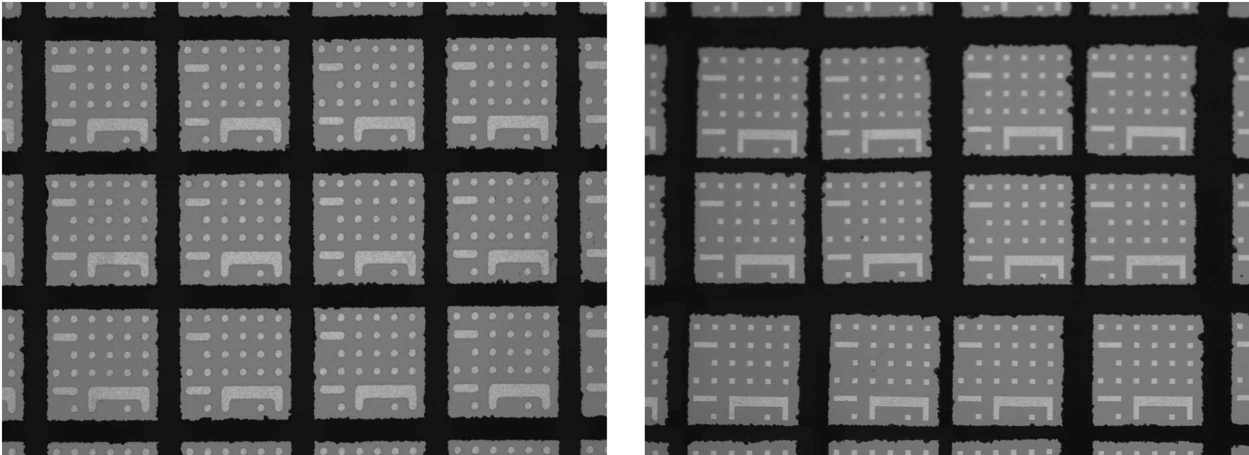


Figure 4.4: Pictures of die-dummies on the UV-tape after dicing. Left: The dies are sitting in a good regular order. Right: The spacing between the die-dummies is unsteady.

A dependence of the pull-off strength on **separation speed** was observed for all types of stamps that had been prepared. Of each type one stamp was chosen and the pull-off strength measured for separation speeds between 0.3 mm/min and 10 mm/min. For all stamps the pull-off strength increased with separation speed by more than a factor of two within this interval (Fig. 4.3). For the design with the small squares (bumps with $300\ \mu\mathrm{m}$ edge length) the maximum pull-off strength reached was 65 kPa for the standard PDMS and 83 kPa for the soft PDMS, reached at a separation speed of 10 mm/min. The maximum pull-off strength measured was 121 kPa, it was reached for the stamp with the big squares design (bumps with 1 mm edge length) made of soft PDMS at a separation speed of 9 mm/min.

4.1.2 transfer printing

Preparation of the samples prior to the transfer printing itself was shown to be a source of inaccuracy. While dicing using a $180\ \mu\mathrm{m}$ wide dicing blade resulted in precise and regular cuts with a width of $200\ \mu\mathrm{m}$, dicing with the slim blade ($35\ \mu\mathrm{m}$ width) was more sensitive. A new blade resulted in a kerf width of $\approx 50\ \mu\mathrm{m}$ and moderate chipping. Cutting one sample of $\approx 1\,\mathrm{cm}^2$ size required $\approx 0.5\,\mathrm{m}$ of cutting length. For the slim blade this led to an increased kerf width of more than $60\ \mu\mathrm{m}$, stronger chipping and the breaking of individual die-dummies after already three to four samples diced. Using the UV-curable dicing tape Adwill D-841 no die-dummies were flushed away during dicing. The strong water flow during dicing led to clean separated die-dummies. However, while the positions of the die-dummies were always unaffected by the dicing the regular order was in some cases destroyed during drying (Fig. 4.4). Proper exposure of the UV-tape and loosening of the die-dummies was essential to obtain reliable pick up. The design of the stamps profile (square or circular bumps) did however not affect the picking process. Picking up the die-dummies worked reliably with a yield of 90% to 100% (Fig. 4.5).
The UV-tape samples with the separated die-dummies allowed the pick-up of 9 complete 7×7

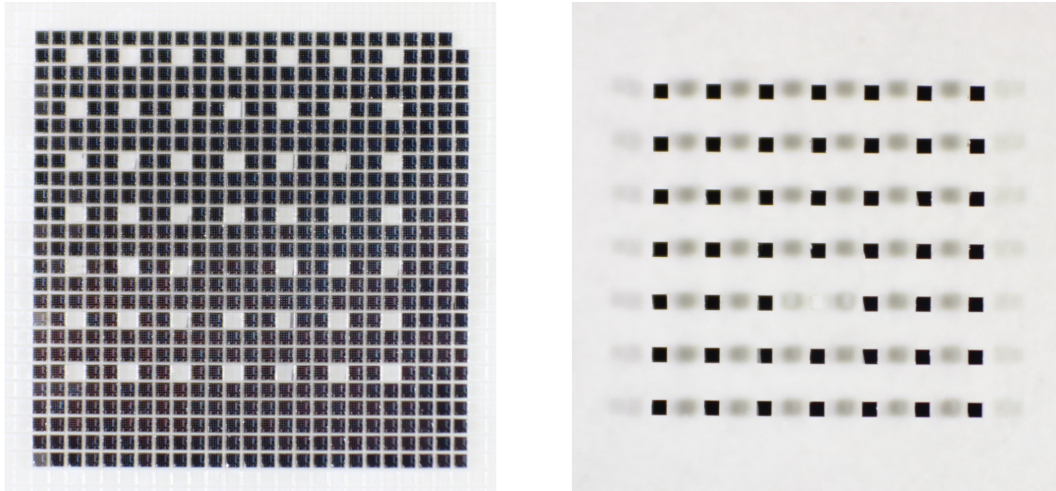


Figure 4.5: Pictures of separated die-dummies on the UV-tape (left) with one array already picked up and transferred to a sugar coated substrate (right). From the 49 die-dummies meant to be transferred 48 have been transferred corresponding to a yield of approx. 98%. No wrong die-dummies have been transferred.

arrays (Fig. 4.6 left). The pick-up of all 9 arrays was performed for two samples resulting in a total yield of 94.6% and 98.9%, respectively. The transfer of the arrays from the stamp to the sugar coated substrate was always successful (i.e. 100% yield). The right picture in Figure 4.6 shows a complete array transferred to a sugar coated substrate.
While a high yield above 90% on average was reached for both stamps made of the normal and the soft PDMS, the selectivity was lower for stamps made of soft PDMS, meaning that it occurred more often, that wrong die-dummies were additionally picked up by the stamp. Often neighboring die-dummies were additionally picked up. They were not transferred in the second transfer from the stamp to the sugar surface, thus this transfer step was selective too. The resulting selectivity for the stamps made of soft PDMS improved, when the profile depth was increased from $100\,\mu\mathrm{m}$ to $150\,\mu\mathrm{m}$.
As standard stamps made of the normal PDMS, with a profile depth of $100\,\mu\mathrm{m}$ and $225\,\mu\mathrm{m} \times 225\,\mu\mathrm{m}$ square bumps were established. The stamps did not alter and were used for several dozen transfer printing processes over a time period of a year.
To examine the accuracy of relative positions of the individual die-dummies in a transferred array pictures were taken under the microscope and superimposed in different ways. For the left picture in Fig. 4.7 the picture of a complete transferred array was superimposed with a regular array of red squares representing the ideal positions of the die-dummies. Thus the picture shows the shift of every die-dummy against its ideal position. For the right picture in Fig. 4.7 the picture of a complete transferred array was superimposed with a by 90° rotated, contrast inverted copy of itself.
While in some cases individual die-dummies showed strong rotation and/or shift from their ideal position, for the majority of the die-dummies a maximum shift of approximately $10\,\mu\mathrm{m}$ to $15\,\mu\mathrm{m}$ was observed.

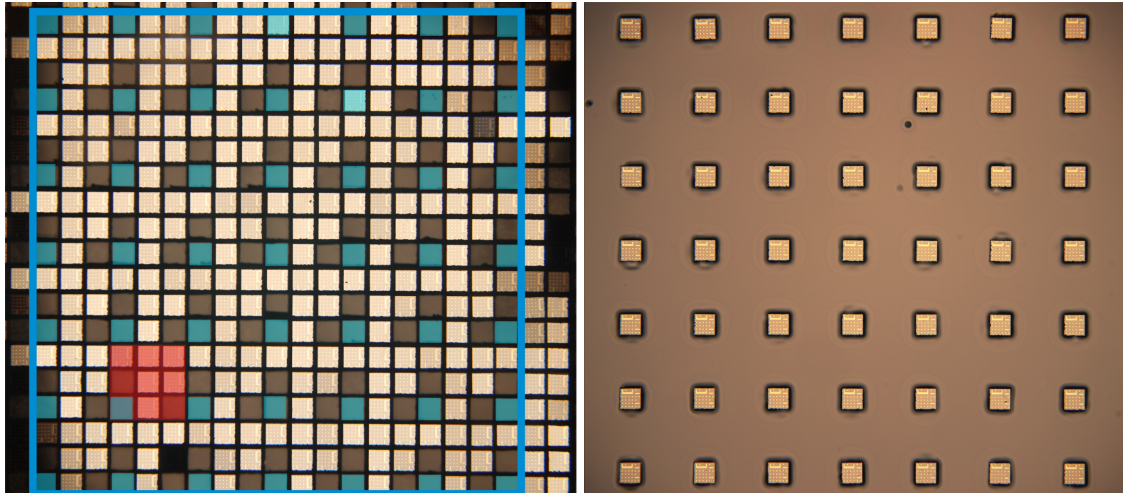


Figure 4.6: Left: Picture of separated die-dummies on UV-tape. Three arrays have already been picked up from the sample. The blue frame marks one array, with the 49 sites of the array highlighted (blue squares). On two of the highlighted sites the die-dummy was not picked up. The red square emphasizes a "unit cell" of the nine arrays that can be picked up from the sample. Right: Complete 7×7 array of die-dummies transferred to a sugar coated substrate.

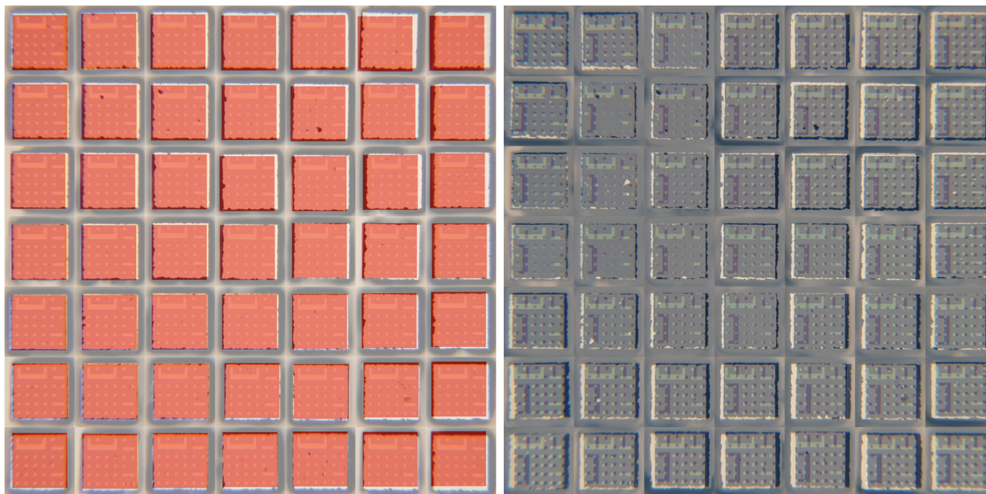


Figure 4.7: Collages of a transferred 7×7 array highlighting the accuracy of relative die positions after the transfer. The collages were compiled from the original pictures by cutting out the empty areas of the shown array, keeping only those parts of the picture showing the elements of the array. Left: The picture of the transferred array was overlain with a regular array of ($250\ \mu\text{m} \times 250\ \mu\text{m}$) sized red squares representing the ideal positions of the dies. Right: The picture of the transferred array was overlain with a by $90°$ rotated contrast inverted copy of itself. White and black areas indicate imperfect overlap, which is a sign for misalignment.

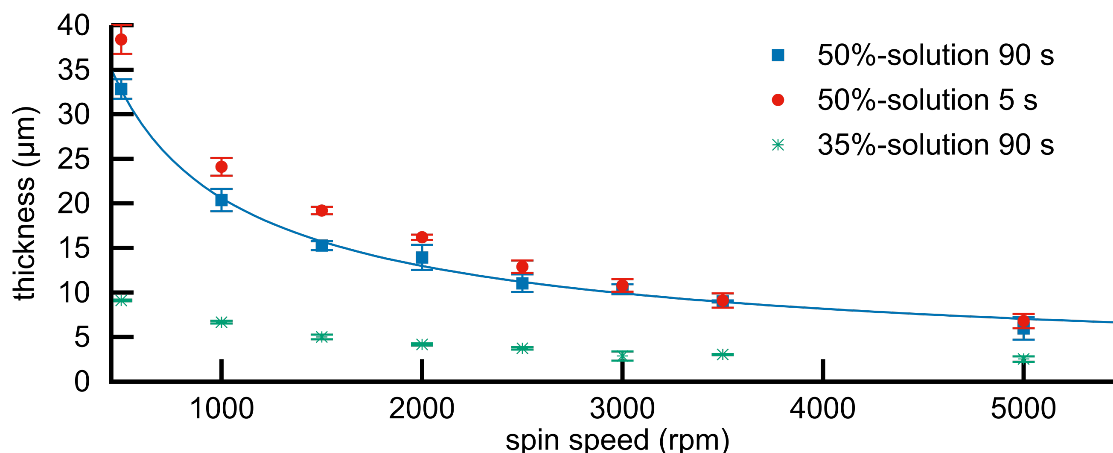


Figure 4.8: Spin curves for a 50 wt-% solution of shellac in ethanol spun for 90 and 5 seconds, and for a 35 wt-% solution of shellac in ethanol spun for 90 seconds.

4.2 embedding of dies

The embedding process itself resulted in a homogeneous PDMS layer with the die-dummies embedded. Careful execution could completely avoid the trapping of air bubbles. The thickness of the PDMS was as dictated by the used spacers which could be the same thickness as the die-dummies (210 µm) or thicker (e.g. 550 µm).
The separation of the one glass substrate, when the PDMS was cured, worked reliably also for a thickness of the shellac of only approximately 2 µm. Afterwards the shellac could completely be washed away, releasing a clean surface.
Figure 4.8 gives the spin curves for a 50 wt-% and a 35 wt-% solution of shellac in ethanol. The resulting layer thickness at 2500 rpm was approximately 3.7 µm for the 35 wt-% solution and 11 µm for the 50 wt-% solution. However, while the surface of the cured shellac films were smooth, they were uneven on a larger scale, comprising a waviness of $W_a \approx 800$ nm (arithmetic mean deviation) for a film coated with 2500 rpm from 50 wt-% solution and a waviness of $W_a \approx 80$ nm (arithmetic mean deviation) for a film coated with 2500 rpm from 35 wt-% solution. Also the layer thickness was inhomogeneous towards the edge of the substrate.
The resulting surface topography after the embedding process was determined in the turning step prior to the pouring in PDMS when the array was flipped by transferring it from the sugar coated substrate to a shellac coated glass substrate. This process first attached the substrate with the sugar coating to a second substrate covered by a shellac film. In the second part of the process the stack was divided by dissolving the sugar with water. For the first part different routes have been tried entailing different results. However, if both substrates were attached to the array, the second part of the process never caused problems.
The surface topography of the samples after the embedding process was measured using a profilometer[1]. Usually the die-dummies protruded from the resulting surface by several micrometers and showed deep trenches looking like convex menisci at the edges of the

[1]Dektak XT, Bruker, USA

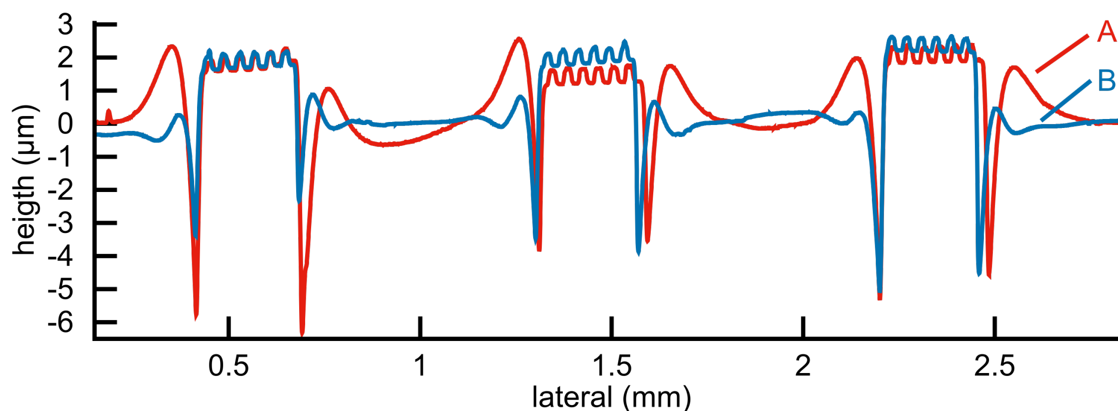


Figure 4.9: Topography of the surface of two different samples after embedding, measured using a profilometer. For both samples the turning step was conducted by dropping the substrate with the array into the shellac, heated to 100°C. A: The shellac film was prepared from 50 wt-% solution using a spin speed of 5000 rpm for 20 s. B: The shellac film was prepared from 50 wt-% solution using a spin speed of 2500 rpm for 90 s.

embedded die-dummies (Fig. 4.9). Figure 4.10 shows 3D mapscans of the surface of different samples performed with the profilometer. For each sample an area of $500\,\mu\text{m} \times 500\,\mu\text{m}$ around an embedded die-dummy was scanned. The notable differences in the maximum height differences and the meniscus like feature at the edge of the die-dummies can be seen. While the die-dummy in Fig. 4.10 (a) clearly protrudes from the surface, it is nearly at one level with the surrounding surface in Fig. 4.10 (c) and builds a cavity in Fig. 4.10 (b). The meniscus-like trench is very pronounced for the die-dummy of the sample in (c) and small in (b) and (d) of Fig. 4.10.

The turning step, flipping the array prior to the embedding process, could be changed in three ways affecting the resulting surface topography of the sample after embedding in PDMS: the procedure to bring the two samples into contact, the thickness of the shellac film and how the shellac film was made sticky.

To bring the sugar coated wafer piece into contact with the prepared shellac coated sample two routes have been followed. For the first route the samples were brought to contact using the fineplacer and the sugar coated sample holding the array was pressed into the shellac with a force of approximately 2 N to 3 N. This process was not very reliable and often part of the array was not transferred to the shellac. In this case some of the rows starting from one side of the array were transferred and the remaining rows to the opposite side of the array were lost when the wafer piece substrate was detached by dissolving the sugar coating in water. The surface topography for samples where this turning procedure was applied showed a gradient in how much the die-dummies protruded from the surface (Fig. 4.11). Towards the side of the array where rows have been lost during the turning step the die-dummies protruded less.

For the second route the sugar coated wafer piece holding the array was placed about 1 mm above the shellac with the fineplacer and then dropped to the prepared shellac film. This process was much more reliable and no gradient in how much the die-dummies protrude from the surface was observed (Fig. 4.9).

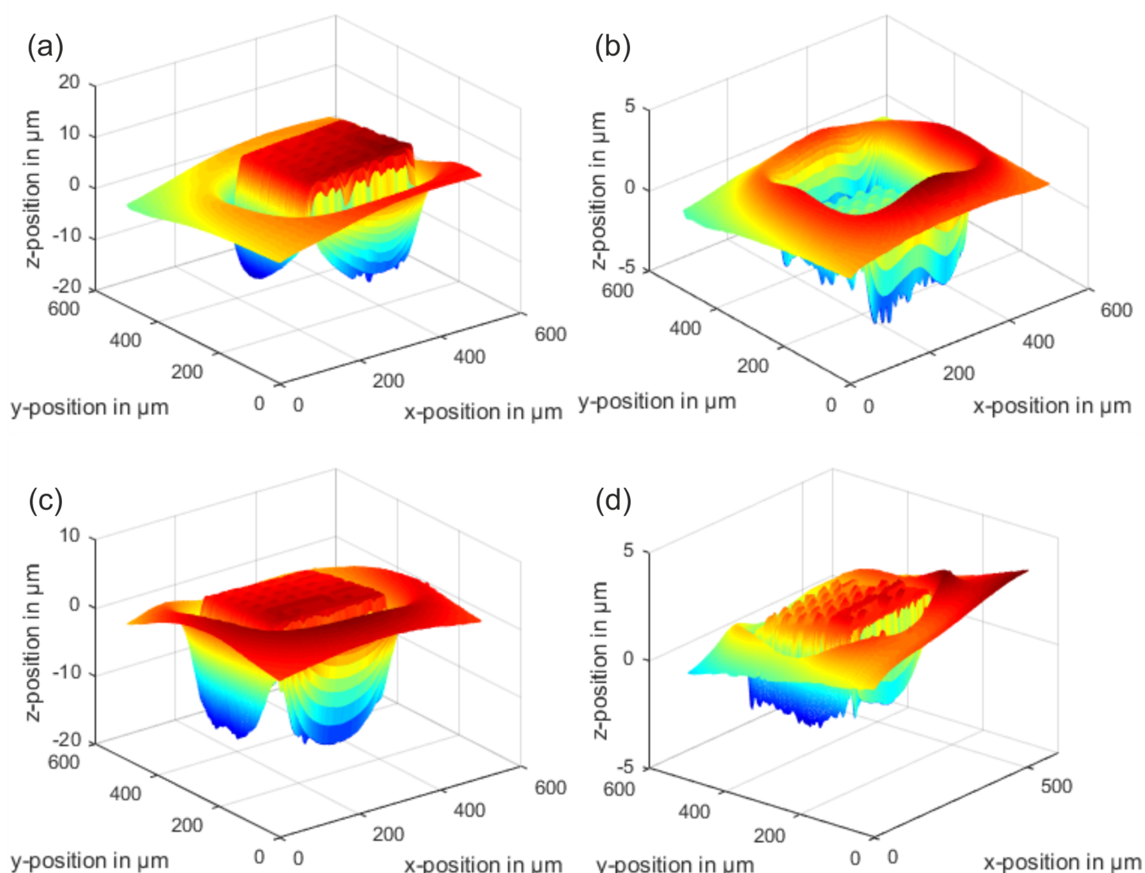


Figure 4.10: 3D map scans of embedded die-dummies measured using a profilometer. The samples differ in how the shellac film was prepared and at what temperature the turning step was performed. (a) The shellac was spin coated using a spin speed of 5000 rpm. The substrate with the array was dropped into the uncured shellac film, before it was heated to 120°C. (b) The shellac was spin coated using a spin speed of 5000 rpm. The cured film was heated to 100°C before the substrate with the array was dropped into it. (c) The shellac was spin coated using a spin speed of 3000 rpm. The cured film was heated to 110°C before the substrate with the array was dropped into it. (d) The shellac was spin coated using a spin speed of 3000 rpm. The cured film was heated to 120°C before the substrate with the array was dropped into it.

The thickness of the shellac film determined the maximum height by which the die-dummies protruded from the surface after embedding. However, the exact surface topography depended more on how the shellac film was softened or, to be more general, made sticky, which was essential for a successful turning step. Three paths have been followed for this purpose.

Dropping the array into the uncured shellac film directly after spin coating the solution on the substrate, curing the film while the sample with the array attached to it, resulted in a very reliable turning step with a high yield, without loss of individual die-dummies. However, the resulting surface topography at the end of the embedding process showed large height differences up to $\approx 40\,\mu m$ (50 wt-% solution, 5 s with 3000 rpm spinning speed). The convex menisci like features at the edge of the die-dummies were very pronounced.

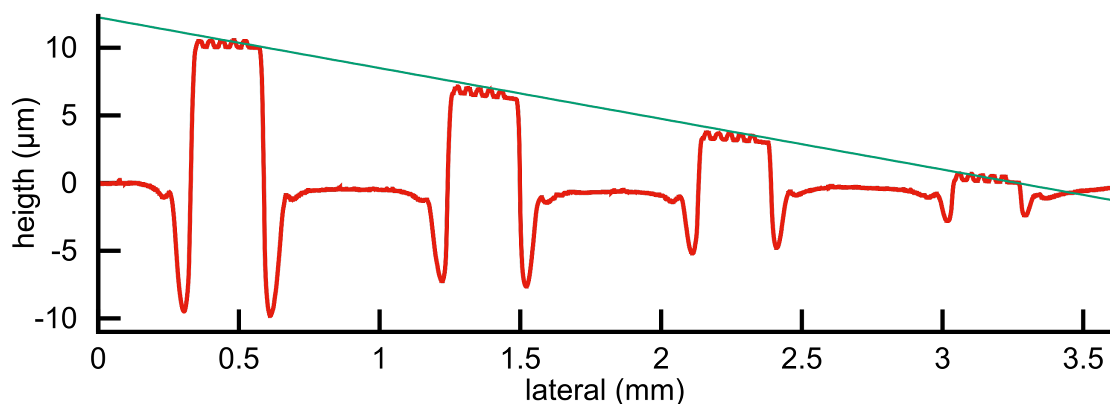


Figure 4.11: Topography of the surface after embedding, measured using a profilometer. During the turning step, the substrate with the array was pressed into the shellac with $\approx 2\,\mathrm{N}$. The slope of the line corresponds to a tilt of $\approx 0.21°$ against the horizontal.

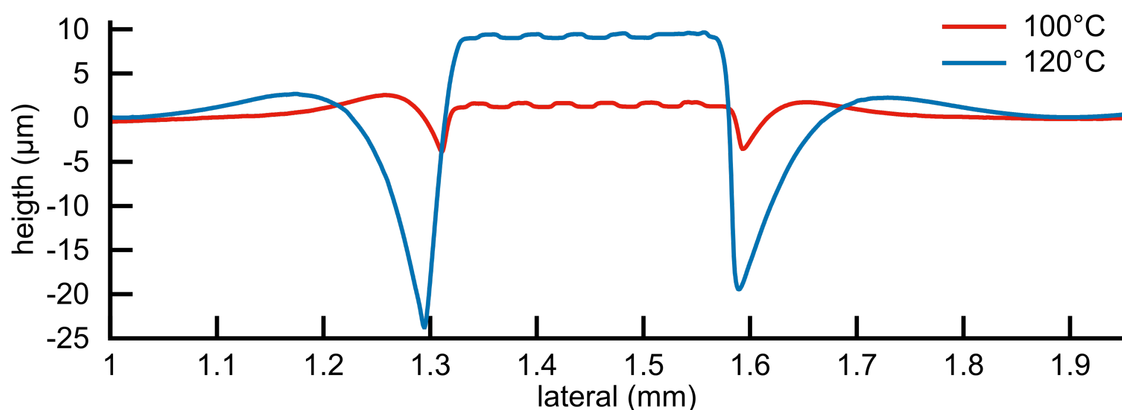


Figure 4.12: Topography of the surface of two different samples after embedding, measured using a profilometer. The turning step was performed with a temperature of 100°C for one sample and with a temperature of 120°C for the other sample. Both samples show a negative meniscus at the edge of the die-dummy. However, the sample where the turning step was performed with a temperature of 100°C shows less height differences.

Solvating the shellac film on its surface by exposing the cured shellac film to an ethanol atmosphere in principle worked and resulted in less topography, but the process showed low reproducibility. It was not possible to determine an adequate duration for the process to reliably achieve a sufficient sticky surface. If the surface was exposed to the ethanol atmosphere too briefly, the surface was not sticky enough, and the turning process was accompanied by the loss of die-dummies. A longer exposure however led to more surface topography at the end of the embedding process.
The last path followed to prepare the shellac film for the turning step was softening the shellac by thermal heating. Reproducibility was not a problem for this process. While the shellac itself

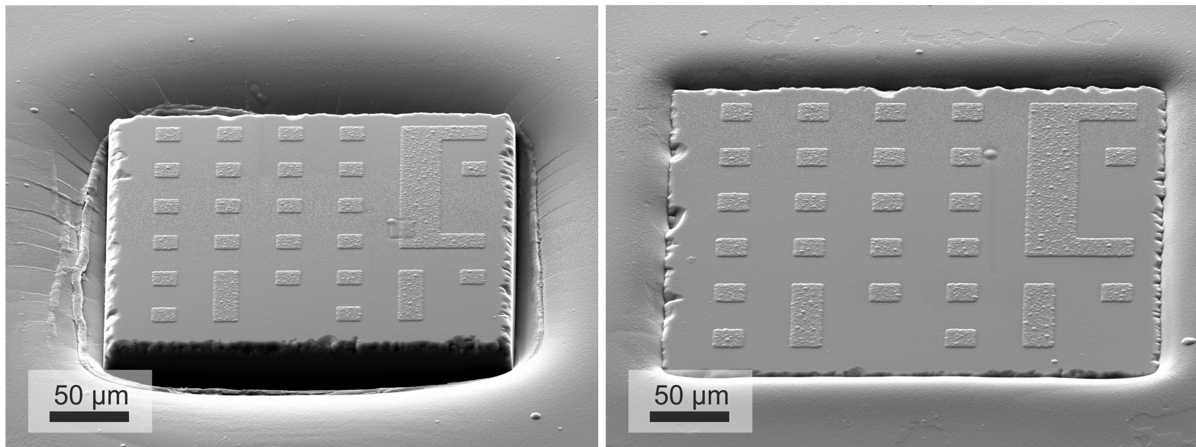


Figure 4.13: SEM-pictures of embedded die-dummies. Both pictures show different die-dummies on the same sample. The shellac film was prepared from 50 wt-% solution using a spin speed of 5000 rpm for 20 s. The turning step was performed by dropping the array to the shellac film heated to 120°C. Around the die-dummy in the left picture the surface forms a deep trench and the vertical side-walls of the die-dummy are partly exposed. Around the die-dummy in the right picture the surface is almost flat and no step occurs at the edge of the die-dummy.

started to soften at approximately 80°C the turning process did not work with the film heated to this temperature and was not reliable at a temperature of 90°C. It was however reliable for temperatures of 100°C and above. The resulting surface topography after embedding increased in amplitude with increasing temperature during the turning step (Fig. 4.12), but was very small for temperatures up to 100°C (Fig. 4.15 right).
So, while different procedures and parameters during the turning step determined the resulting surface topography, the resulting surface could never be predicted for sure. Sometimes the surface did look different at different positions in the array (Fig. 4.13). Sometimes unexpected an almost flat surface was obtained (left picture in Fig. 4.14).

4.3 fabrication of electrical connections

The lithographic steps for the fabrication of electrical connections were shown to be possible but challenging, thus the simple application of standard processes for the etching of VIAs or the structuring of conducting tracks was not possible.

4.3.1 fabrication of VIAs

The fabrication of the first layer of VIAs required the alignment of a photomask on the dies of the array. Alignment was possible, while usually not perfect. Overlap of the mask structures with the corresponding structures on the dies could be achieved for most of the dies of an array, while the overlap for a majority of the dies was only partial (Fig. 4.16).
The fabrication of the VIAs using a negative resist mask (process (a) in Fig. 3.10) resulted in the formation of cracks in the parylene surface. The cracks formed in the resist during

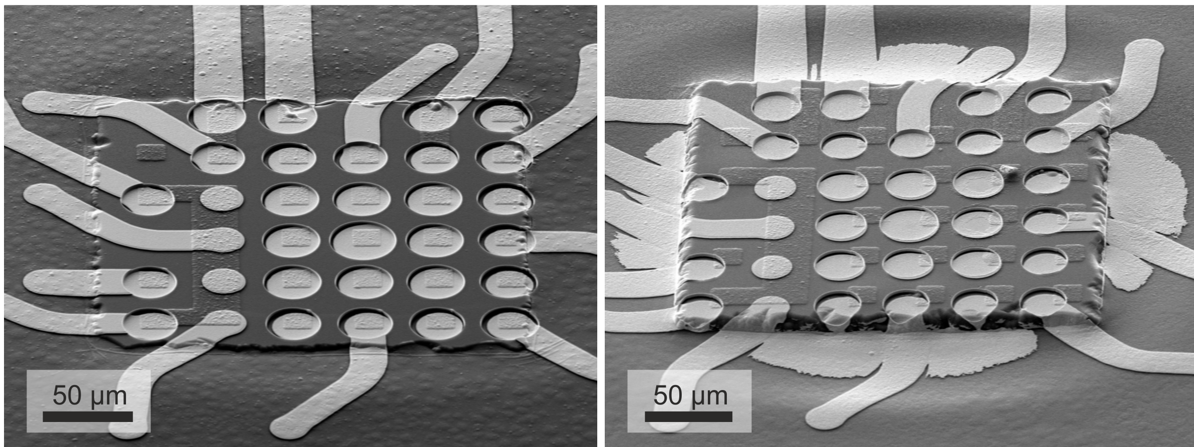


Figure 4.14: SEM-pictures of embedded die-dummies with the first VIA-layer and the first layer of conducting tracks already fabricated on top. For both samples the turning step has been performed using a shellac film spin coated from 50 wt-% solution using a spin speed of 3000 rpm for 5 s, which was made sticky at its surface by exposing it to an ethanol atmosphere. Left: The surface is almost flat. Right: The die-dummy protrudes $\approx 10\,\mu\mathrm{m}$ from the surface. Around the die-dummy the surface forms a smooth trench, where the gold of the conducting tracks was not structured properly.

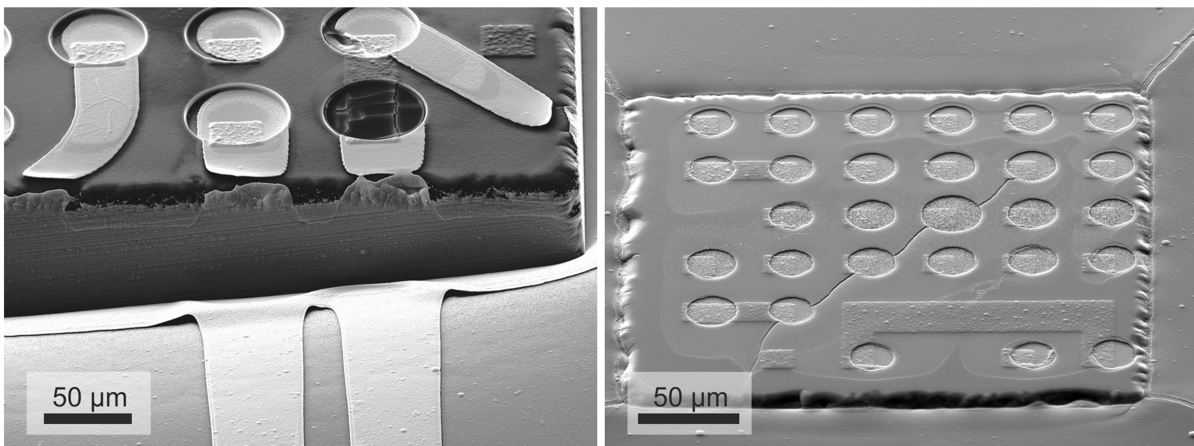


Figure 4.15: Left: SEM-picture of the edge of an embedded die-dummy of a sample where the first VIA-layer and the first layer of conducting tracks have already been fabricated on top. The turning step prior to the embedding process was performed with an uncured shellac film. The surface drops more than $30\,\mu\mathrm{m}$ at the edge of the die-dummy. While the side-walls of the die-dummy are covered with gold, the tracks can not follow the $90°$ angle at the edge and are interrupted. Also the gold is not structured in the trench after the edge. Right: SEM-picture showing a single die-dummy after embedding and the fabrication of the first VIA layer using a chromium hartmask. The turning step has been performed using a shellac film spin coated from 50 wt-% solution using a spin speed of 3000 rpm for 5 s, which was heated to $90°$C. The surface is almost flat with the die-dummy protruding only by several $1\,\mu\mathrm{m}$. The chromium has led to cracks in the parylene surface.

evacuation in the RIE machine. They where very fine when they formed, but became wider during etching. Also they originally only formed in the resist and were then transferred to the

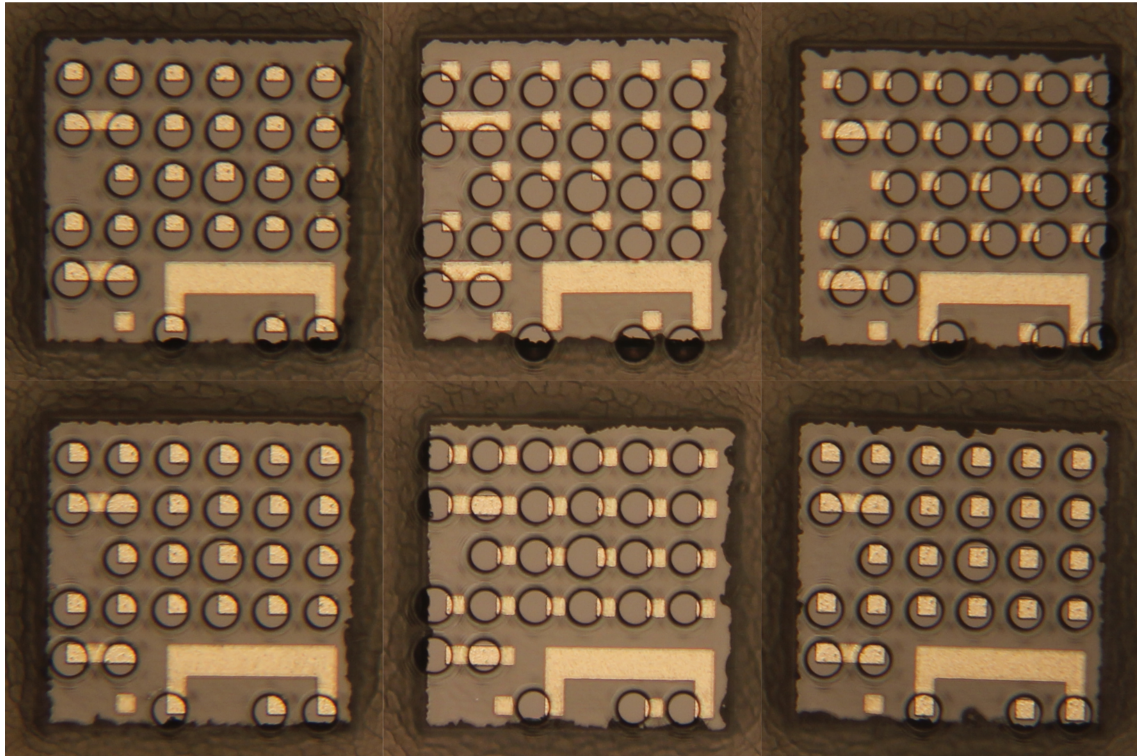


Figure 4.16: Light microscope pictures of six neighboring die-dummies of an embedded array. The first layer of VIAs has already been fabricated on top (circles). The alignment fits well for the two die-dummies of the left column and the lower right die-dummy. For the remaining die-dummies there is only partial respectively no (upper center) overlap between VIAs and contact pads.

parylene during etching. The cracks only formed for the samples with the parylene on top of the PDMS. Reducing the thickness of the PDMS underneath the parylene (by reducing the thickness of the spacers from > $500\ \mu m$ to $200\ \mu m$) did not prevent the formation of cracks. Cutting the resist and the parylene near the edge with a scalpel to allow movement of the different layers and to relieve stress also did not hinder the formation of the cracks.
Etching of the parylene using a positive resist mask and a dark field mask (process (c) in Fig. 3.10) also resulted in the formation of cracks in the parylene surface, although less cracks formed than with the negative resist process.
The fabrication of the VIAs by etching against a hardmask (process (b) in Fig. 3.10) was accompanied by the nontransparent hardmask material (aluminum and chromium were used) being between the dies of the array and the mask. However, due to surface topography and the surface structure of the dies their contours where visible through the hardmask and thus alignment of the mask on the dies of the array was possible.
Chromium sputtered onto the surface of the samples directly led to the formation of numerous cracks starting at all dies of the array and running through the complete surface. However, etching of the chromium worked reliably.
The aluminum did not lead to the formation of any cracks. When the VIAs of the first VIA layer were completely etched before the hardmask was removed, the contact pads of the die-dummies

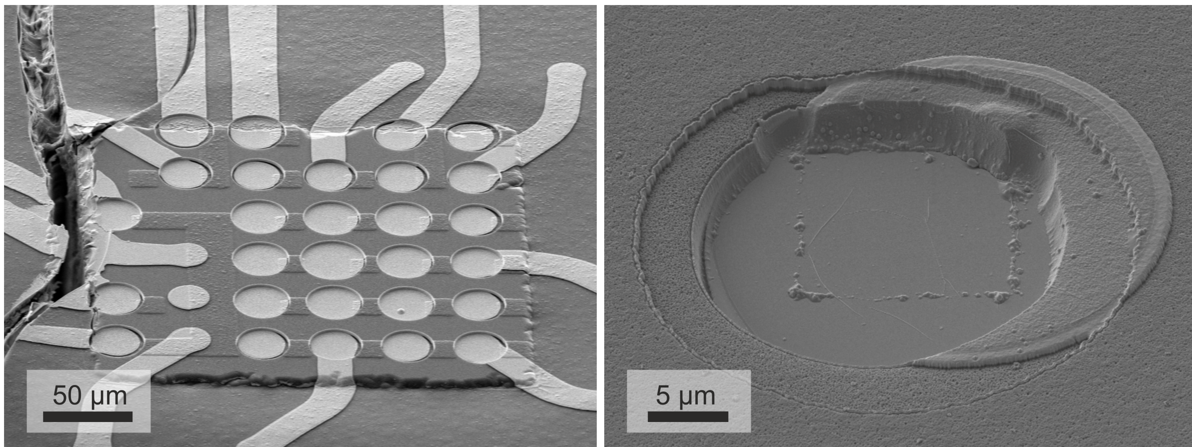


Figure 4.17: Left: SEM-picture of an embedded die-dummy with the first layer of VIAs and the first layer of conducting tracks fabricated on top. On the left side of the die-dummy a crack in the surface passes by interrupting all conducting tracks crossing it. Right: SEM-picture of a VIA fabricated using an aluminum hardmask and a Ti/Au/Ti circle of the first layer of conducting tracks. Only the contour of the aluminum pad of the die-dummy is visible, as it was etched away, when the hardmask was removed.

were exposed to the etching solution during removal of the hardmask. For the die-dummies with contacts pads made of aluminum the contact pads were thus also etched away (Fig. 4.17 right). For the samples with die-dummies having contact pads made of chromium the fabrication of the VIAs using an aluminum hardmask worked fine.
The flanks of the etched VIAs were not vertical, but rather steep.

4.3.2 fabrication of conducting tracks

With the alignment marks from the first lithographic fabrication steps (fabrication of VIAs) alignment was not an issue during the fabrication of the conducting tracks (Fig. 4.18 left). The deposited Ti/Au/Ti film did not always look homogeneous prior to structuring, which was attributed to surface roughness after the fabrication of the VIAs, resulting from etching processes and the exposure to different solvents.
Cracks in the surface formed during the fabrication of the VIAs proved to be insurmountable obstacles interrupting any tracks crossing them (Fig. 4.17 left).
Depending on the result of the embedding process and the given surface topography the edges of the dies could form obstacles too. While the metalization could cross steps of few μm when the dies protruded (Fig. 4.14 right), for too big step sizes the tracks tended to be interrupted at the edge where they had to follow a $90°$ bend (Fig. 4.15 left).
The formation of a trench around the dies could result in the metalization not being structured there (Fig. 4.14 right). This led to a round halo-like closed gold film around the dies (Fig. 4.18 right). It could be shown, that this was caused by the resist mask not being fully structured (Fig. 4.19). Longer exposure times (twice as long) could not reliably improve the result and too long exposure bore the risk of reducing the resolution of the process and thus leading to improper structuring too. Longer exposure times did not always affect the result in the expected way,

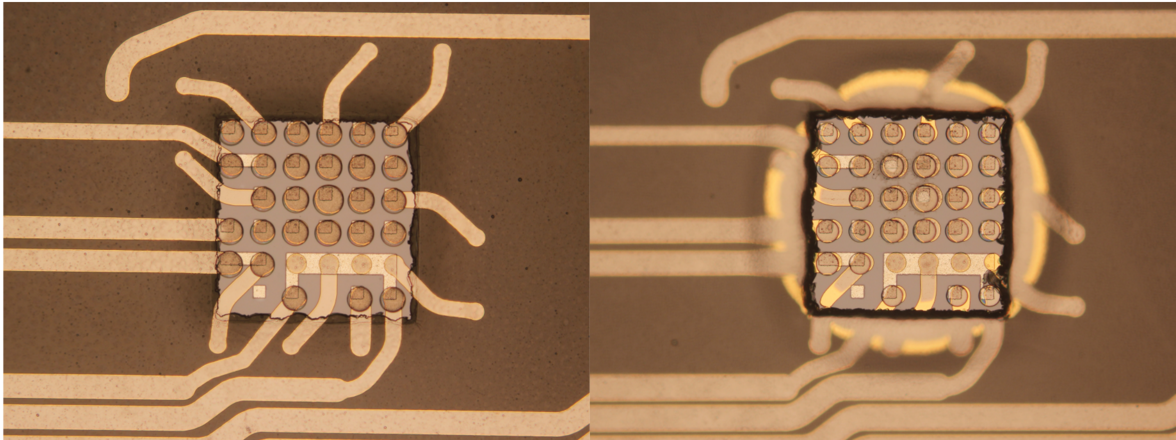


Figure 4.18: Light microscope pictures of one die-dummy of an array embedded with the first VIA layer and the first layer of conducting tracks fabricated on top. Left: VIAs and conducting tracks are well aligned. The conducting tracks traverse the edge of the die-dummy without disturbance. Right: Small misalignment between VIAs and tracks. Around the die-dummy the surface forms a deepening. Inside this deepening the gold has not been structured during the fabrication of the tracks and hence all tracks leaving the die-dummy are short-circuited.

leading to the assumption that the optimal exposure time strongly depends on the surface of the individual sample. The surface of the samples can be more or less reflecting depending on its roughness resulting from previous fabrication steps.

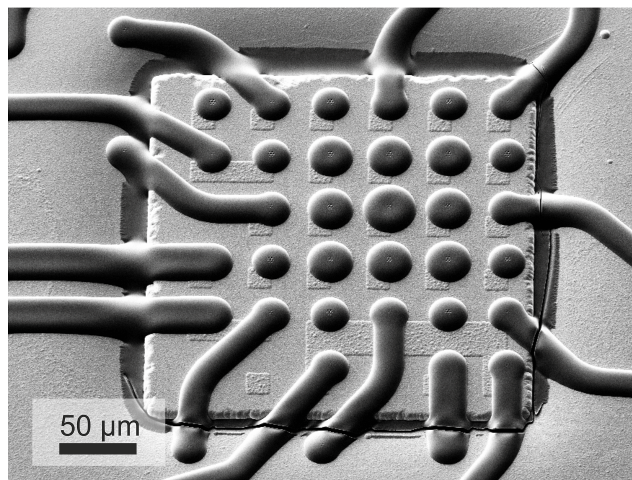


Figure 4.19: SEM picture of an embedded die-dummie. A Ti/Au/Ti film was sputter deposited onto the surface, before a resist mask was structured. The resist is structured properly except for a slim resist frame around the die-dummy where the surface forms a trench.

4.4 mechanical properties of the foil-system

The envisioned chip-in-foil system has been modeled as a multilayer stack consisting of different materials with different Young's moduli. The main part of the system is a bilayer stack of parylene C and PDMS. In some areas of the system the PDMS is replaced by the dies and thus silicon. Further, additional barrier layers might be added to the system.
For all calculations the following values for the Young's moduli of the different materials have been used: $E_{\text{parylene}} = 2.8\,\text{GPa}$ [2], $E_{\text{PDMS}} = 1.32\,\text{MPa}$ [79], $E_{\text{silicon}} = 131\,\text{GPa}$ [3] and $E_{\text{Al2O3}} = 195.3\,\text{GPa}$ [175].
The position of the neutral axis, where during bending no strain occurs, was calculated for different material stacks. Table 4.1 provides the calculated positions of the neutral axis z_1 from the top surface for the different layer systems.

Table 4.1: The position of the neutral axis z_1 (from the top surface) for different material stacks.

	Al_2O_3	parylene C	Al_2O_3	PDMS	silicon 2	z_1
system 1	-	12 µm	-	210 µm	-	6.91 µm
system 2	-	12 µm	-	525 µm	-	11.43 µm
system 3	-	14 µm	-	210 µm	-	7.79 µm
system 4	-	12 µm	-	190 µm	-	6.75 µm
system 5	-	12 µm	-	-	210 µm	116.86 µm
system 6	0.02 µm	12 µm	0.02 µm	210 µm	-	6.76 µm
system 7	0.02 µm	12 µm	-	210 µm	-	6.21 µm
system 8	-	12 µm	0.02 µm	210 µm	-	7.44 µm
system 9	0.1 µm	12 µm	-	210 µm	-	4.48 µm

For a stack consisting of 12 µm of parylene C on top of 210 µm PDMS (system 1 in Tab. 4.1) the neutral axis is located 6.91 µm from the top surface and thus in the middle of the parylene C layer. For a stack composed of parylene C and silicon e.g. "system 5" in Tab. 4.1 the neutral axis is in the middle of the silicon.
For "system 1" (first row Tab. 4.1) the maximum strain occurring on the upper surface $\varepsilon_{\text{max1}}$ and the lower surface $\varepsilon_{\text{max2}}$ has been calculated in dependence of the radius of curvature r of a cylinder the system is wrapped around (Fig. 4.20). In the considered configuration the top surface of the system is on the outside, and thus the neutral axis is $r + z_2$ from the center of the cylinder. While the upper surface becomes stretched, the lower surface is compressed and thus the strain is negative. For a radius of curvature of $0.5\,\text{mm}$ the maximum strains are: $\varepsilon_{\text{max1}} \approx 0.966\%$ and $\varepsilon_{\text{max2}} \approx 30.079\%$. Bending the system in the other direction, with the top surface of the system touching the cylinder, leads to a changed bending radius at the neutral axis of $r + z_1$. Thus the occurring maximum strains at the surfaces are changed to $\varepsilon_{\text{max1}} \approx 1.363\%$ at the parylene surface and $\varepsilon_{\text{max2}} \approx 42.432\%$ at the PDMS surface.

[2] *Parylene specifications and properties*, Specialty Coatings Systems (2003)

[3] `https://www.korth.de/index.php/material-detailansicht/items/32.html` (June 2, 2019)

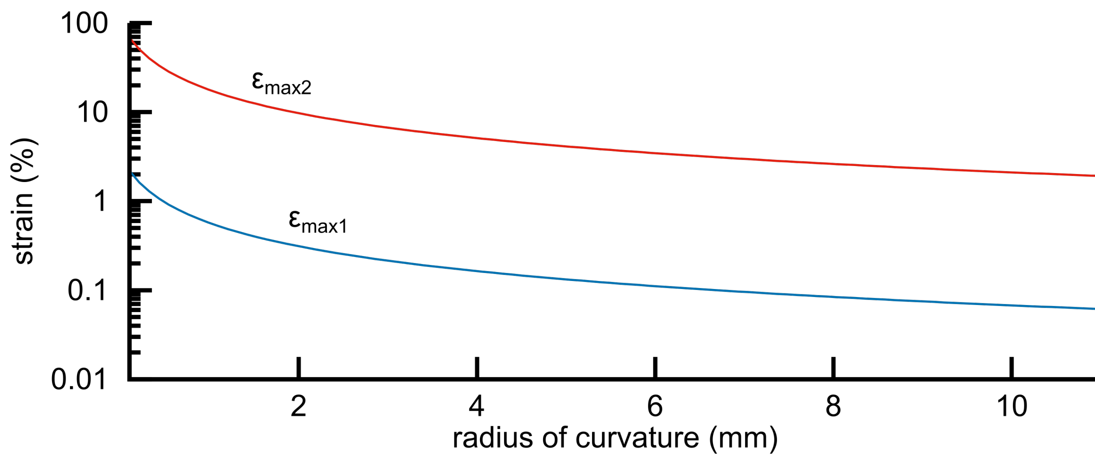


Figure 4.20: The maximum strain at the top ($\varepsilon_{\text{max1}}$) and bottom ($\varepsilon_{\text{max2}}$) surface of “system 1” for different bending radii.

If the thickness of the PDMS in a parylene C/PDMS bilayer is decreased by $20\,\mu\text{m}$ (“system 1” to “system 4”) the maximum strains during bending with a radius of curvature of 0.5 mm are slightly changed: $\varepsilon_{\text{max1}} \approx 0.971\%$ and $\varepsilon_{\text{max2}} \approx 28.084\%$, respectively. Further, the neutral axis moves away from the parylene C/PDMS interface. The strain difference at the top surface of the two systems is -0.005% and becomes zero approximately $1.1\,\mu\text{m}$ under the surface. Near the neutral axis the difference is approximately 0.023%. On the lower surface of “system 4” the difference is approximately 0.802%.
While the strain changes linearly through the cross-section of the multilayer stacks, the stress jumps at the interfaces and is accompanied by different slopes in the different materials.
For a cross-section of the system of approximately $5\,\text{cm} \times 250\,\mu\text{m}$ a load corresponding to 1 kg results in stress of $\approx\ 0.8\,\text{MPa}$. A stress of 0.8 MPa applied to “system 1” results in approximately 0.52% of strain. The same stress applied to “system 4” – accompanied by a 9% smaller cross-sectional area – results also in an approximately 9% lower strain of 0.48%. For “system 5”, where the PDMS is replaced by silicon, 0.8 MPa of stress would result in $7 \cdot 10^{-5}\%$ strain.

4.5 characterization of ALD layers

4.5.1 electrical characterization

Al_20_3

The equivalent circuit model (Fig. 3.13) was fitted to each impedance spectrum to gain the capacitance of the measurement field, which allowed then the calculation of the relative permittivity ε of the ALD layer. Table 4.2 shows the mean values and standard deviations for the specific capacitance (capacitance per area) and ε for different samples. The values obtained

Table 4.2: Values for the specific capacitance and relative permittivity of Al_2O_3 films of different thickness d. The values are obtained by modeling an equivalent circuit to the impedance spectra. Each row belongs to another sample, rows separated by a solid line are from different deposition runs.

machine	d (nm)	GPC (nm)	C $\left(\frac{\text{nF}}{\text{mm}^2}\right)$	ε
MyPlas	26.7	0.19	2.76 ± 0.05	8.33 ± 0.16
MyPlas	26.7	0.19	2.83 ± 0.07	8.52 ± 0.20
MyPlas	48.4	0.17	1.61 ± 0.07	8.81 ± 0.40
MyPlas	48.4	0.17	1.60 ± 0.04	8.73 ± 0.23
MyPlas	72.1	0.17	1.22 ± 0.07	9.89 ± 0.58
MyPlas	38.2	0.15	1.95 ± 0.07	8.40 ± 0.29
Oxford	33.1	0.16	2.37 ± 0.08	8.86 ± 0.30
Oxford	33.1	0.16	2.31 ± 0.05	8.64 ± 0.20

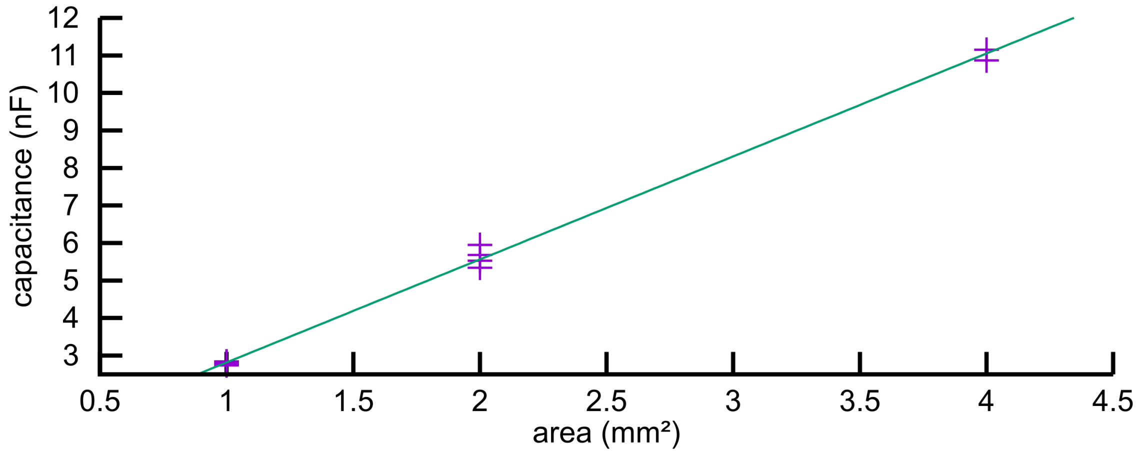


Figure 4.21: Capacitance in dependence of the area of the measurement field for 26.7 nm of Al_2O_3. The line was fitted to the data points.

for the relative permittivity were in the range between 8.05 and 10.42.

Each sample contained measurement fields with areas of 1, 2 and 4 mm^2. For the two samples of the first two rows in Table 4.2 (coming from the same deposition run) all individual capacitances obtained from the fitted equivalent circuit have been plotted against the area of the individual measurement fields (Fig. 4.21). A line was fitted to the points providing a slope of $2.75\,\frac{\text{nF}}{\text{mm}^2}$ and an offset of 0.07 nF.

The current behavior over time was measured for a 48.4 nm thick film, after the applied voltage was increased from 0 to 1 V (see Fig. 4.22). For the first 100 seconds the current decreases approximately with $\frac{1}{\text{t}}$, then the type of decay changes an becomes exponential. The curve fitted to the data from 100 seconds to 200 seconds decays $\propto e^{-a \cdot t}$ with a $\approx 0.013\,\text{s}^{-1}$.

Leakage currents were then measured by increasing the voltage in steps of 0.05 V every 240 s. The length of the steps was set to allow decay of the high charging current at the beginning while keeping a reasonable measurement time. The current value was always stored immediately

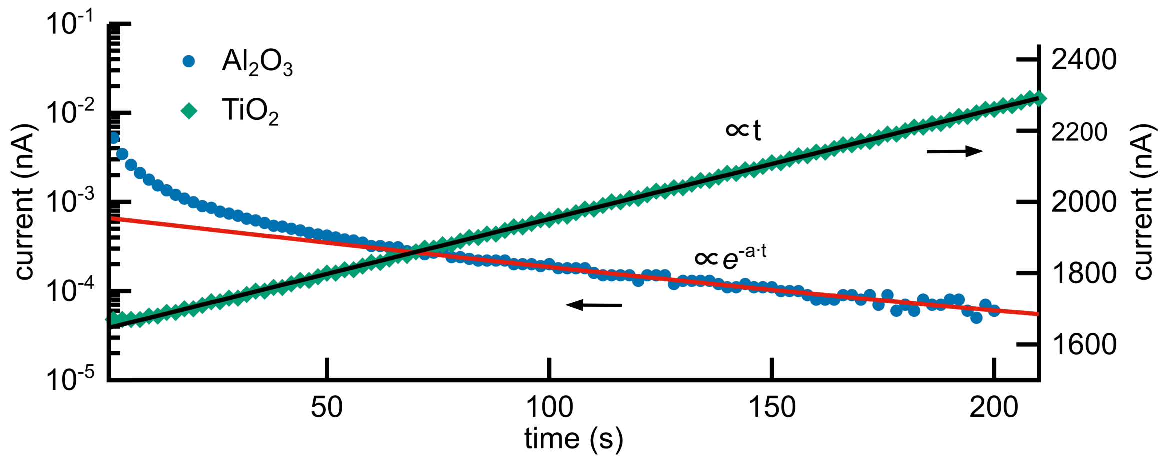


Figure 4.22: Current over time after a voltage step from 0 to 1 Volt, on a 48.4 nm thick Al_2O_3 film (left hand axis) and a 43.5 nm thick TiO_2 film (right hand axis).

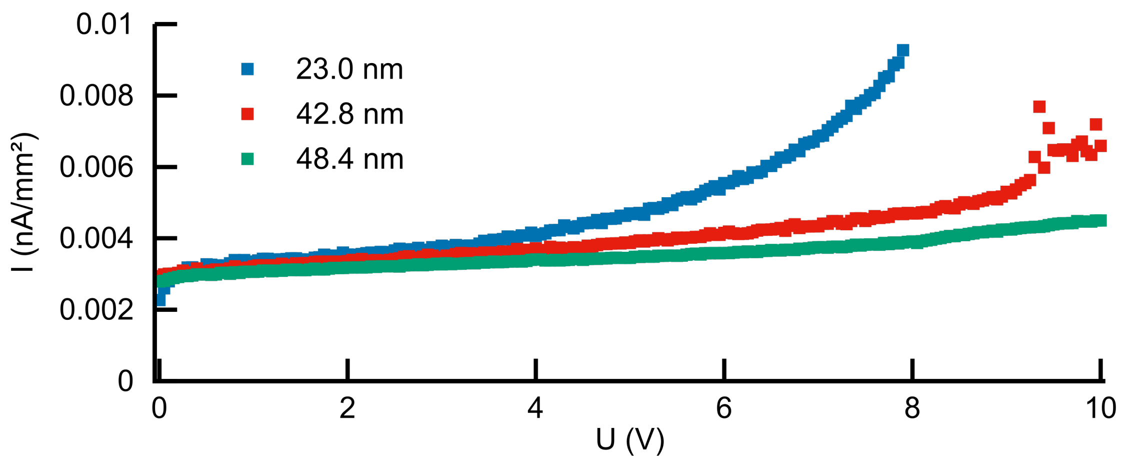


Figure 4.23: Leakage current density of three different Al_20_3 films, all deposited using the *MyPlas*.

before the next voltage step. A current of 0.03 nA that was measured as current offset of the measurement unit at 0 V was added to all measured currents. The measured current over voltage curves allow comparison of different layers. Figure 4.23 shows the leakage current of three different layers of 23.0 nm, 42.8 nm and 48.4 nm thickness. The leakage current is in the range of 10^{-3} nA/mm^2 and starts rising for voltages above 5 V for the 23.0 nm thick layer and for voltages above 9 V for the thicker layers.

To measure the dielectric strength the voltage was increased in steps of 0.5 V every 2 s. Breakdown was recognized either in the current-voltage diagram or due to light flashes. Table 4.3 provides all measured dielectric strengths. All obtained values were in the range between 4.5 and 8.6 MV/cm.

Table 4.3: Obtained dielectric strength values for different $Al_2 0_3$ films. U_{break} gives the mean value of the voltage, were breakdown occurred. All mean values and standard deviations are based on the number N of measurements given in the last column.

machine	d (nm)	U_{break} (V)	dielectric strength (MV/cm)	N
MyPlas	23.0	15.90 ± 0.86	6.91 ± 0.37	5
MyPlas	26.7	15.58 ± 1.64	5.84 ± 0.62	6
MyPlas	38.2	32.83 ± 0.24	8.60 ± 0.06	3
MyPlas	42.8	30.83 ± 0.24	7.20 ± 0.06	5
MyPlas	48.4	35.21 ± 3.84	7.28 ± 0.79	7
MyPlas	72.1	48.75 ± 0.74	6.76 ± 0.10	3
Oxford	24.8	14.25 ± 1.25	5.75 ± 0.50	2
Oxford	26.3	14.75 ± 1.75	5.61 ± 0.67	2
Oxford	33.1	25.64 ± 0.23	7.75 ± 0.07	7

Table 4.4: Values for the specific capacitance and relative permittivity of TiO_2 films from different deposition runs. The values are obtained by modeling an equivalent circuit to the impedance spectra. Each row belongs to another sample, rows separated by a solid line are from different deposition runs.

process	d (nm)	GPC (nm)	C $\left(\frac{\text{nF}}{\text{mm}^2}\right)$	ε
MyPlas, plasma, 100°C	28.7	0.053	10.67 ± 0.17	34.57 ± 0.57
MyPlas, plasma, 100°C	28.7	0.053	10.83 ± 0.15	35.09 ± 0.48
MyPlas, plasma, 100°C	29.9	0.060	9.28 ± 0.19	31.33 ± 0.71
MyPlas, plasma, 100°C	38.0	0.052	7.57 ± 0.23	32.49 ± 0.97
MyPlas, plasma, 100°C	38.0	0.052	7.96 ± 0.11	34.15 ± 0.49
MyPlas, plasma, 100°C	43.5	0.044	6.94 ± 0.19	34.09 ± 0.94
MyPlas, plasma, 100°C	43.5	0.044	7.38 ± 0.45	36.27 ± 2.21
MyPlas, plasma, 100°C	63.0	0.042	4.53 ± 0.06	32.22 ± 0.41
MyPlas, plasma, 100°C	63.0	0.042	4.48 ± 0.07	31.89 ± 0.52
Oxford, plasma, 120°C	30.7	0.040	9.70 ± 0.53	33.63 ± 1.84
Oxford, plasma, 300°C	36.6	0.046	13.31 ± 0.93	55.03 ± 3.84
Oxford, plasma, 300°C	36.6	0.046	11.19 ± 0.19	46.26 ± 0.78
Oxford, thermal, 300°C	89.2	0.032	11.87	119.58

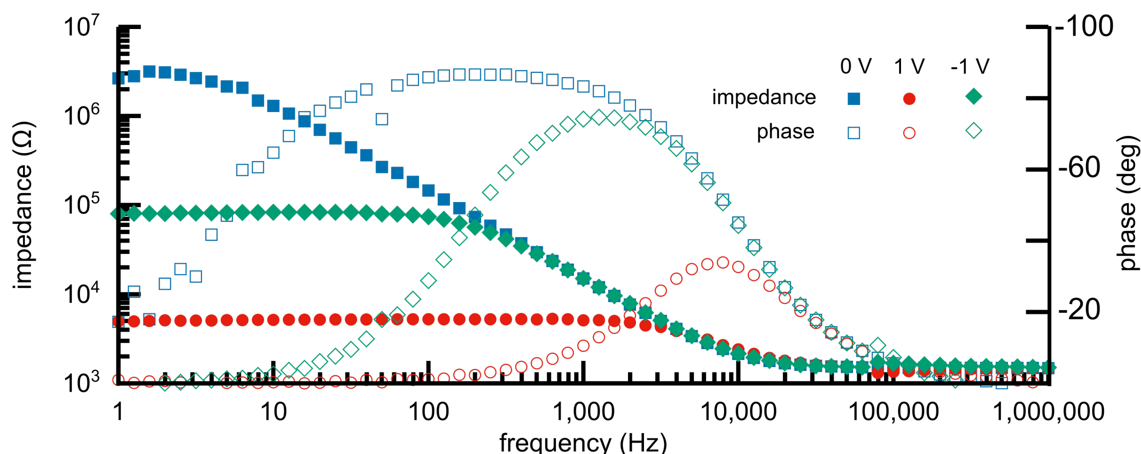


Figure 4.24: Impedance spectra of a 28.7 nm thick TiO_2 film deposited in the *MyPlas*. The spectra were taken without, as well as with a +1 V and a -1 V voltage offset, respectively.

TiO_2

For the TiO_2 films the specific capacitance was also obtained from fitting the equivalent circuit model to the impedance spectra. It was used to calculate the relative permittivity of the films (Tab. 4.4). For all films deposited in a plasma-enhanced process at 100°C respectively 120°C the obtained relative permittivity was in the range between 33.63 and 35.59. For the films deposited in the plasma-enhanced process at 300°C substrate temperature values between 44.97 and 58.12 for the relative permittivity were obtained. For the samples with the films deposited in a thermal ALD process at 300°C short-circuits in the measurement fields allowed only the measurement of one measurement field, resulting in a value of $\varepsilon \approx 120$.

Impedance spectra were also measured with voltage offsets of ± 1 V, resulting in changed spectra with respect to the original impedance spectrum measured with 0 V DC offset. The impedance dropped at low frequencies. The drop depended on the sign of the voltage offset. This effect was observed for all measured TiO_2 films independent of the substrate temperature during deposition. Figure 4.24 shows the impedance spectra for a 28.7 nm thick TiO_2 film deposited in the *MyPlas* at a substrate temperature of 100°C.

As in the case of the Al_2O_3 films, prior to leakage current measurements the current was measured over time after the voltage was increased from 0 to 1 V. Figure 4.22 shows the measurement obtained for a 43.5 nm thick film deposited at 100°C in the *MyPlas*. The fitted line has a slope of 3.1 nA/s. For a 63 nm thick film deposited using the same process a current decay could be observed within the first 80 seconds after the applied voltage step. Afterwards the current rose up to a factor of 1000 when the measurement was stopped after more than 20 hours.

Leakage current was measured by increasing the voltage in steps of 0.1 V every 5 seconds and measuring the current value immediately before the next voltage step. The length of the voltage step was decreased compared to the measurements on the Al_2O_3 films due to the observed linear rise of the current with time (Fig. 4.22) after only very short decay. As several samples showed

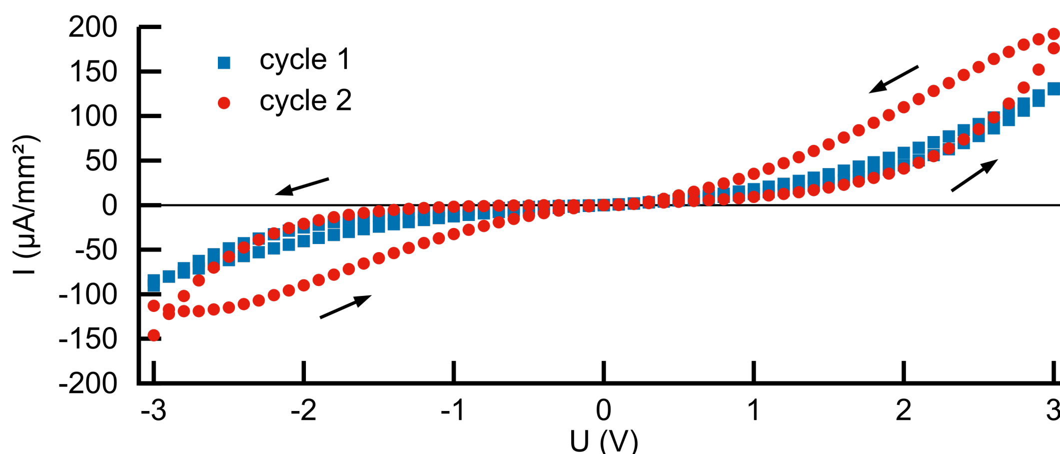


Figure 4.25: Leakage current of a 63 nm thick TiO_2 film deposited in a plasma-enhanced process at 100°C substrate temperature. The voltage was swept from -3 V to +3 V to -3 V two times. The voltage was changed in steps of 0.1 V every 5 seconds.

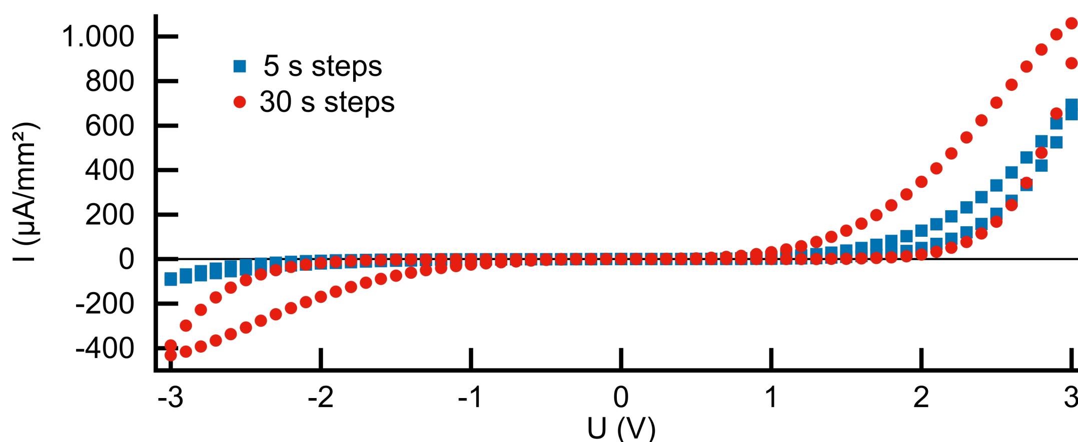


Figure 4.26: Leakage current of a 38 nm thick TiO_2 film deposited in a plasma-enhanced process at 100°C substrate temperature. The voltage was changed in steps of 0.1 V every 5 respectively 30 seconds.

rectifying behavior, i.e. the current amplitude depended on polarity of the applied voltage, the voltage was swept repeatedly, linearly from -3 to +3 V and back.
For voltages below 1 V leakage currents were in the range of $1\ \mu A/mm^2$. For a voltage of 3 V leakage currents increased to several $100\ \mu A/mm^2$.
The films deposited in plasma-enhanced processes at either 100°C or 120°C showed no or only little rectifying behavior, but a current hysteresis. Figure 4.25 shows the leakage current of a 63 nm thick TiO_2 film deposited in a plasma-enhanced process at 100°C substrate temperature using the *MyPlas*. The voltage was swept from -3 to +3 V and back twice. While the first cycle resulted in only small current hysteresis, the second cycle led to a distinct current hysteresis. The film shows no rectifying behavior.

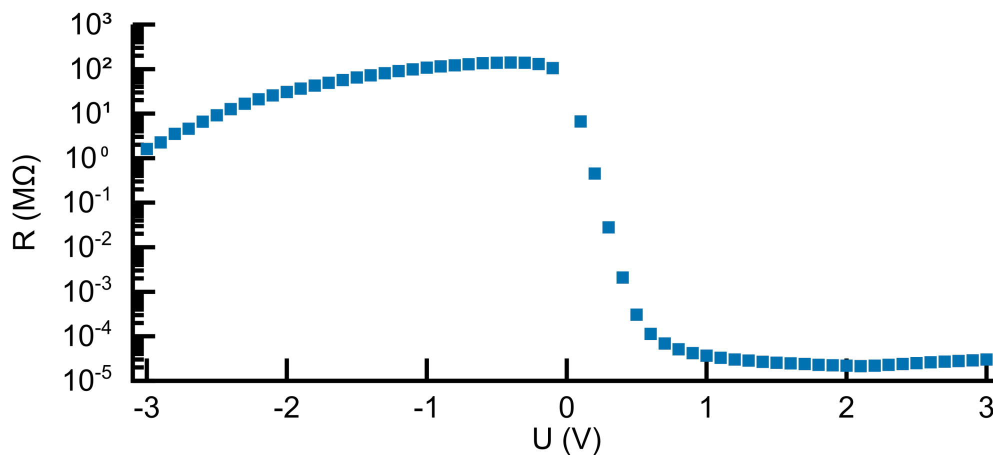


Figure 4.27: The ratio $R=U/I_{leak}$ for a 89.2 nm thick TiO_2 film deposited in a plasma-enhanced process at 300°C substrate temperature.

Figure 4.26 shows the leakage current of a 38 nm thick TiO_2 film deposited in a plasma-enhanced process at 100°C substrate temperature using the *MyPlas*. The voltage was swept twice. In the first sweep the duration of the voltage steps was 5 s each. In the second sweep the duration of the voltage steps was increased to 30 s leading to a more pronounced current hysteresis. The film shows rectifying behavior.
Strong rectifying behavior but no hysteresis was observed for films deposited in a plasma-enhanced process at 300°C substrate temperature. Figure 4.27 shows the calculated ratio $R=U/I_{leak}$ for a 89.2 nm thick TiO_2 film deposited at 300°C substrate temperature. While the resistance for positive voltages is approximately 10 Ω, it is above 10 MΩ for negative voltages.

multilayers

The thickness of Al_2O_3/TiO_2 multilayers could not be measured directely and was therefore calculated from the number of cycles and the GPCs of the individual layers. The total thickness of the deposited multilayers was always about 100 nm.
According to the monolayers an equivalent circuit model was fitted to the impedance spectra in order to obtain the specific capacitance of the layers. An effective relative permittivity was then calculated, which was the relative permittivity a single material of same thickness must have to show the same specific capacitance as the multilayer (Tab. 4.5).
Electrical breakdown occurred at voltages between 43 V and 74 V. The mean values for the dielectric strength of the differently composed multilayers are depicted in Table 4.6.

Table 4.5: Specific capacitance and an effective relative permittivity for Al_2O_3/TiO_2 multilayers of different compositions.

machine	layer composition	C $\left(\frac{nF}{mm^2}\right)$	$\varepsilon_{\text{effective}}$
MyPlas	$5 \times (100\,\text{cycles}_{\text{TMA}} + 100\,\text{cycles}_{\text{TTIP}})$	1.12 ± 0.06	12.99 ± 0.75
MyPlas	$5 \times (100\,\text{cycles}_{\text{TMA}} + 100\,\text{cycles}_{\text{TTIP}})$	1.17 ± 0.03	13.53 ± 0.32
MyPlas	$2 \times (200\,\text{cycles}_{\text{TMA}} + 300\,\text{cycles}_{\text{TTIP}})$	1.28 ± 0.06	13.39 ± 0.65
MyPlas	$2 \times (200\,\text{cycles}_{\text{TMA}} + 300\,\text{cycles}_{\text{TTIP}})$	1.31 ± 0.07	13.64 ± 0.74
MyPlas	$3 \times (135\,\text{cycles}_{\text{TMA}} + 200\,\text{cycles}_{\text{TTIP}})$	1.29 ± 0.06	13.55 ± 0.76
MyPlas	$3 \times (135\,\text{cycles}_{\text{TMA}} + 200\,\text{cycles}_{\text{TTIP}})$	1.28 ± 0.07	13.52 ± 0.68
Oxford	$5 \times (100\,\text{cycles}_{\text{TMA}} + 100\,\text{cycles}_{\text{TTIP}})$	1.37 ± 0.07	14.33 ± 0.74
Oxford	$5 \times (100\,\text{cycles}_{\text{TMA}} + 100\,\text{cycles}_{\text{TTIP}})$	1.38 ± 0.05	14.64 ± 0.50

Table 4.6: Voltage U_{break} where electrical breakdown occurred and dielectric strength for Al_2O_3/TiO_2 multilayers of different compositions. N refers to the number of measurements the mean values and standard deviations are based on.

machine	layer composition	U_{break} (V)	dielectric strength (MV/cm)	N
MyPlas	$5 \times (100\,\text{cycles}_{\text{TMA}} + 100\,\text{cycles}_{\text{TTIP}})$	45.19 ± 1.50	4.52 ± 0.15	8
MyPlas	$5 \times (100\,\text{cycles}_{\text{TMA}} + 100\,\text{cycles}_{\text{TTIP}})$	55.15 ± 7.94	5.20 ± 0.75	4
MyPlas	$5 \times (100\,\text{cycles}_{\text{TMA}} + 100\,\text{cycles}_{\text{TTIP}})$	71.13 ± 2.19	6.94 ± 0.21	4
MyPlas	$2 \times (200\,\text{cycles}_{\text{TMA}} + 300\,\text{cycles}_{\text{TTIP}})$	59.13 ± 0.54	6.40 ± 0.06	4
MyPlas	$3 \times (135\,\text{cycles}_{\text{TMA}} + 200\,\text{cycles}_{\text{TTIP}})$	58.67 ± 0.85	6.29 ± 0.09	3
Oxford	$5 \times (100\,\text{cycles}_{\text{TMA}} + 100\,\text{cycles}_{\text{TTIP}})$	52.81 ± 7.36	5.62 ± 0.78	8

4.5.2 permeation measurements

The accuracy and reproducibility of the setup were tested by repeated measurements of two reference foils over a period of one week. For the first reference foil a total of 15 measurements resulted in a mean value of $(4.01 \pm 0.24) \cdot 10^{-7}$ mbar · ℓ/s (6% error). For the second reference foil deterioration could be observed after several measurements. However, for the first five measurements a mean value of $(8.62 \pm 0.41) \cdot 10^{-9}$ mbar · ℓ/s (5% error) was obtained. Besides obvious deterioration due to injury of the foil, repeated measurement in general showed no trend. The minimum value that can be measured is determined by the background, that is the value measured when the leak detector is in standby with the valve towards the sample closed. This value could be as low as $5 \cdot 10^{-12}$ mbar · ℓ/s. At the end of a measurement the helium was purged out of the setup with nitrogen. However, the background value increased and settled at a higher value around $1 \cdot 10^{-10}$ mbar · ℓ/s or higher, when many measurements were performed. To be sure that the measured helium leakage was due to diffusion though the foil, and not due to helium bypassing the sample by diffusing though the sealing rings restricting the measurement field, a measurement was performed on a 25 μm thick steel foil, that was expected to be "impermeable". The leak rate detected stayed at its starting point for the approximately first 5 min, then it rose linearly with $2 \cdot 10^{-13} \frac{\text{mbar} \cdot \ell/\text{s}}{\text{s}}$. Concerning the rings glued to the foils it was assured that they did not affect the measurement results. The glue used was highly permeable to helium and thus did not affect the measurement result, even when it covered part of the measurement area.

For each kind of foil, uncoated samples were tested first as reference before coated foils were tested, allowing then the determination of the barrier improvement factor (BIF) due to the coating (i.e. the factor by which the helium leak rate is lower for a coated foil compared to the uncoated reference foil). For the 125 μm thick Kapton foil the measured values for the uncoated foil ranged from $1.3 \cdot 10^{-6}$ mbar · ℓ/s to $7.2 \cdot 10^{-6}$ mbar · ℓ/s and for repeated measurements on the same sample a constant increase in helium leak rate was observed. For the 6 μm thick polyimid foil a value of $1.4 \cdot 10^{-5}$ mbar · ℓ/s was obtained that did not alter during repeated measurements. Parylene C foils of similar thickness in contrast showed increasing values for repeated measurements and the formation of cracks in the foil could be observed. The cracks formed in a circle around the center of the sample where the ground of the measurement area showed a step or gap (e.g. at the rim of the used supporting structure). For foil thicknesses above $\approx$ 10 μm the formation of cracks could be prevented. The quality of the parylene could vary depending on the deposition process and thus the mean value of the helium leak rate multiplied by the foil thickness comes with large error: $(4.32 \pm 0.82) \cdot 10^{-4} \frac{\text{mbar} \cdot \ell\, \mu\text{m}}{\text{s}}$. For foils prepared within the same deposition run there was however less variance.

The Kapton foil was easy to handle and did not require further preparation. To the 6 μm polyimid foils a ring had to be glued to prevent rolling up of the foils after detachment. To detach the foils from the glass handle substrate they were prepared on, they were stored in a water bath at 60°C. Depending on the ALD coating on top of the foil this could last more than two days. Sometimes detachment required careful lifting of the foil at the position of the glued ring e.g. with a scalpel. The long water bath could dissolve ALD coatings, however the layer did not dissolve when the top layer was TiO_2. The parylene foils had to be treated like

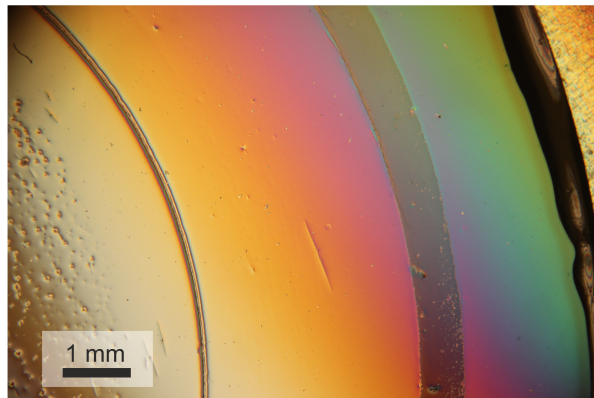


Figure 4.28: Light microscope picture with phase contrast of a parylene foil with ALD coating after measurement. From left to right different features can be observed. At the left side of the picture (center of the sample) the structure of the used supporting structure is molded into the foil. As second feature from left to right a ring follows, where the foil was strongly mechanically stressed and shows micro cracks. This is the position where the supporting structure ends. The last feature is a wide ring at the position of the sealing ring, where the coating is removed from the foil (colorless area). At the right end of the picture part of the metal ring glued to the sample can be seen.

the 6 μm polyimide foils. A resist layer underneath the parylene made the detachement of the foils easier. Still, more than a day and careful mechanical assistance e.g. with a scalpel could be necessary. The measurement of the coated samples resulted always in increasing values for repeated measurements. As there was a distinct trend this could not be attributed to statistical fluctuations of the measurement values, but was a sign for degradation of the samples properties. This was independent of the supporting structure used. However, as any rim and gap was prone to cause damage to the foil, a disc made of steel foil covering the complete measurement area inside the sealing ring was used. This then left only one gap at its rim plus its surface roughness as a source of foil deformation/bending. Surface topography of the support structure markedly affected the foils (except for the thick Kapton foils). After the foils were pressed against the support structure with 1 bar during the measurement the surface structure and topography was cast into the foil (Fig. 4.28). Concerning the rings that were glued to the foils two different types have been used. The first type had an inner diameter of 18 mm and an outer diameter of 30 mm and thus covered the foil at the position where the sealing ring is pressed against the sample. The second type had an inner diameter of 28 mm and an outer diameter of 34 mm and thus was completely outside the measurement field. While the first type protected the sample at the position where the sealing ring is pressed onto the sample, the position of the ring often caused troubles during the release of the foil from the glass substrate and required assistance by hand using a scalpel which then included the risk of damaging the foil. Thus, the second type of ring provided a better chance to detach the foil, while keeping a sufficiently big area in the center undamaged.

Table 4.7 gives measurement values obtained for different foil samples with and without different ALD coatings. For each sample the three values of the measurement repetitions are provided, showing in almost every case an increase with any further measurements and hence decreasing barrier properties.

Table 4.7: Table containing measurement values for the helium leak rate of different foils with different ALD coatings. The three values in each line correspond to three repetitions of the measurement performed and are given in chronological order, as they were obtained. For the samples with the $16.5\,\mu m$ parylene C foil and the ALD coatings, the ALD coating was positioned in the center of the foil near the neutral axis.

foil	ALD coating	helium leak rate (mbar $\cdot \ell/s$)		
Kapton	-	$1.7 \cdot 10^{-6}$	$3.2 \cdot 10^{-6}$	$5.6 \cdot 10^{-6}$
Kapton	-	$3.8 \cdot 10^{-6}$	$4.6 \cdot 10^{-6}$	$5.0 \cdot 10^{-6}$
Kapton	-	$6.2 \cdot 10^{-6}$	$6.6 \cdot 10^{-6}$	$7.2 \cdot 10^{-6}$
Kapton	61 nm Al_2O_3	$6.0 \cdot 10^{-7}$	$1.2 \cdot 10^{-6}$	-
Kapton	62 nm Al_2O_3	$6.8 \cdot 10^{-7}$	$1.2 \cdot 10^{-6}$	-
$6\,\mu m$ polyimide	-	$1.4 \cdot 10^{-5}$	$1.4 \cdot 10^{-5}$	$1.4 \cdot 10^{-5}$
$6\,\mu m$ polyimide	38.7 nm Al_2O_3	$9.8 \cdot 10^{-8}$	$1.3 \cdot 10^{-7}$	$1.6 \cdot 10^{-7}$
$6\,\mu m$ polyimide	40.5 nm Al_2O_3	$2.7 \cdot 10^{-7}$	$5.5 \cdot 10^{-7}$	$6.5 \cdot 10^{-7}$
$6\,\mu m$ polyimide	42.8 nm TiO_2	$7.0 \cdot 10^{-7}$	$1.0 \cdot 10^{-6}$	$1.3 \cdot 10^{-6}$
$6\,\mu m$ polyimide	56.7 nm TiO_2	$1.4 \cdot 10^{-7}$	$3.6 \cdot 10^{-7}$	$7.2 \cdot 10^{-7}$
$6\,\mu m$ polyimide	multilayers	$1.4 \cdot 10^{-8}$	$1.7 \cdot 10^{-7}$	$2.7 \cdot 10^{-7}$
$8.5\,\mu m$ parylene C	-	$5.7 \cdot 10^{-5}$	$5.8 \cdot 10^{-5}$	$5.9 \cdot 10^{-5}$
$12\,\mu m$ parylene C	-	$3.0 \cdot 10^{-5}$	$3.1 \cdot 10^{-5}$	$3.2 \cdot 10^{-5}$
$16.5\,\mu m$ parylene C	-	$2.6 \cdot 10^{-5}$	$2.6 \cdot 10^{-5}$	$2.7 \cdot 10^{-5}$
$17.1\,\mu m$ parylene C	-	$2.6 \cdot 10^{-5}$	$2.6 \cdot 10^{-5}$	$2.7 \cdot 10^{-5}$
$24\,\mu m$ parylene C	-	$1.3 \cdot 10^{-5}$	$1.3 \cdot 10^{-5}$	$1.4 \cdot 10^{-5}$
$16.5\,\mu m$ parylene C	multilayers “5/15/5”	$2.0 \cdot 10^{-8}$	$5.1 \cdot 10^{-8}$	$7.4 \cdot 10^{-8}$
$16.5\,\mu m$ parylene C	multilayers “5/15/5”	$2.1 \cdot 10^{-8}$	$1.2 \cdot 10^{-7}$	$2.4 \cdot 10^{-7}$
$16.5\,\mu m$ parylene C	multilayers “5/15/5”	$9.0 \cdot 10^{-9}$	$1.9 \cdot 10^{-8}$	$2.8 \cdot 10^{-8}$
$16.5\,\mu m$ parylene C	multilayers “5/15/5”	$5.2 \cdot 10^{-8}$	$2.7 \cdot 10^{-7}$	$5.6 \cdot 10^{-7}$
$16.5\,\mu m$ parylene C	multilayers “5/30/5”	$9.3 \cdot 10^{-8}$	$5.2 \cdot 10^{-7}$	$5.0 \cdot 10^{-7}$
$16.5\,\mu m$ parylene C	multilayers “5/30/5”	$7.2 \cdot 10^{-8}$	$1.4 \cdot 10^{-6}$	$1.6 \cdot 10^{-6}$
$16.5\,\mu m$ parylene C	multilayers “5/30/5”	$1.2 \cdot 10^{-8}$	$1.5 \cdot 10^{-8}$	$2.9 \cdot 10^{-8}$
$16.5\,\mu m$ parylene C	multilayers “5/30/5”	$1.4 \cdot 10^{-9}$	$2.7 \cdot 10^{-9}$	$3.9 \cdot 10^{-9}$

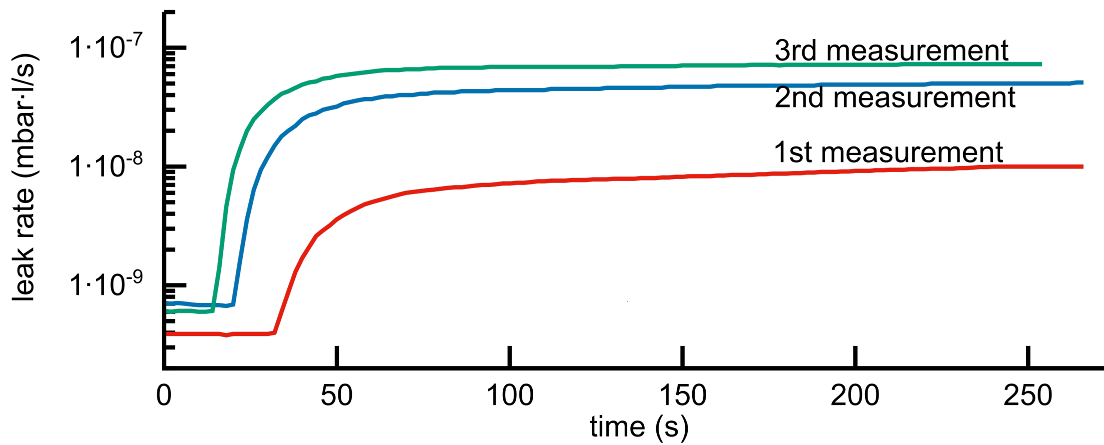


Figure 4.29: Measurement curves for a parylene C/ALD/parylene C foil stack. The two parylene C layers were $8.4\ \mu m$ and $8.1\ \mu m$ thick. The ALD coating was a stack of 5 nm TiO_2/ 15 nm Al_2O_3 / 5 nm TiO_2. The measurement was repeated three times, and the saturation value of the helium leak rate increased from measurement to measurement.

While the Kapton foil was easy to handle it did show worsening properties also in the the case without any ALD barrier coating. The $6\ \mu m$ thick polyimide foil resulted in a constant and reproducible helium leak rate of $1.4 \cdot 10^{-5}$ mbar $\cdot\ \ell/s$. The value did not change for repeated measurements. Additional ALD barrier coatings resulted in decreased helium leak rates with BIFs up to 1000 during the first measurement that then strongly decreased to only ≈ 52 for the third measurement of the sample. This high BIF was reached for an Al_2O_3/TiO_2 multilayer consisting of five bilayers of 15 nm Al_2O_3 and 5 nm TiO_2. The BIFs of single Al_2O_3 or TiO_2 layers were in the range between 20 and 150 during the first measurement, however decreased to 10 to 90 during the third measurement.
For thin parylene C foils below $8\ \mu m$ thickness repeated measurements could result in an increasing helium leak rate, however thicker foils $> 10\ \mu m$ thickness and careful handling resulted in constant values for repeated measurements on the same foil. For samples consisting of two parylene C layers with a total thickness of $16.5\ \mu m$ a helium leak rate of $2.6 \cdot 10^{-5}$ mbar $\cdot\ \ell/s$ was obtained. Additional ALD coatings in the center of the samples between the two parylene C layers resulted in decreased helium leak rates. Three different ALD layer stacks were deposited:

- "5/15/5" multilayers: 5 nm TiO_2/15 nm Al_2O_3/5 nm TiO_2
- "5/30/5" multilayers: 5 nm TiO_2/30 nm Al_2O_3/5 nm TiO_2
- "multilayers": $5\times$(5 nm TiO_2/15 nm Al_2O_3)/5 nm TiO_2

Detaching the foils from their glass handle substrates after the rings were glued to them was delicate and ended in many cases with the samples being visibly damaged. Better results were achieved for samples with a sacrificial resist layer underneath the foil stack. For samples with the ALD "multilayers" the release of the foil system was never successful, and therefore

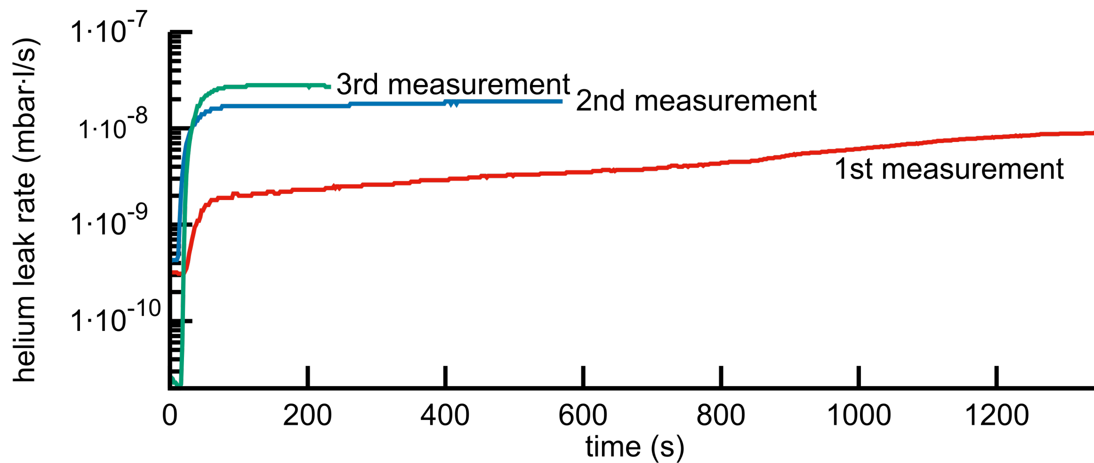


Figure 4.30: Measurement curves for a parylene C/ALD/parylene C foil stack. The two parylene C layers were $8.4\,\mu m$ and $8.1\,\mu m$ thick. The ALD coating was a stack of $5\,nm$ TiO_2/ $15\,nm$ Al_2O_3 / $5\,nm$ TiO_2. The measurement was repeated three times and the saturation value of the helium leak rate increased from measurement to measurement. For the first measurement no saturation was reached, but the value continued to slowly increase with a slope of approximately $9 \cdot 10^{-12}\,\frac{\text{mbar} \cdot \ell/\text{s}}{s}$.

no measurements could be performed for samples of this type. The BIF for all measured (undamaged) samples was in the range between 279 and 18,571 for the first measurement and in the range between 16 and 6,667 for the third measurement.

The observed increase of the measured helium leak rate for repeated measurements was less than for the other samples, where the ALD coating was not at the neutral axis of the foil. However, still a distinct increase could be observed (Fig. 4.29).

While saturation of the helium leak rate during measurement was usually reached after approximately 3 minutes (Fig. 4.29), for the samples consisting of a parylene/ALD/parylene stack the first measurement often did not reach saturation within 15 minutes but the helium leak rate continued to slowly increase (Fig. 4.30). This slow increase was not constant, but changed slope after approximately 12 minutes. For every further measurement saturation was reached within few minutes again. The best measurement values were obtained for a sample with the $5\,nm$ TiO_2/$30\,nm$ Al_2O_3/$5\,nm$ TiO_2 ALD coating. While the first measurement resulted in an value of $1.4 \cdot 10^{-9}$ mbar $\cdot\, \ell/s$ the third value still resulted in a value of $3.9 \cdot 10^{-9}$ mbar $\cdot\, \ell/s$ and thus the value did increase by less than a factor of 3.

Still, less than 25% of the samples initiated could be finished (especially detached) without damage and thus the number of measured samples is low. The resulting measurement values for samples of same type differed and thus a differentiation of samples with different ALD coatings due to the measurement values is not possible.

4.6 fabrication of the Neuroflexarray

All fabrication steps required for the fabrication of the Neuroflexarray – individually described in the sections above – have been combined to fabricate the demonstrator system. This system contained the functionless die-dummies (with chromium contact pads) instead of functioning dies, but required the same fabrication steps. Also the layout was similar to that of the Neuroflexarray with real dies.
The complete fabrication process for the system was very complex and required more than 20 working days. It includes: separation of the dies, transfer printing, embedding, fabrication 1st VIA layer , fabrication 1st layer of conducting tracks, fabrication 2nd VIA layer, fabrication 2nd layer of conducting tracks and fabrication 3rd VIA layer. The individual processes have been described in detail in the previous sections and are by themselves complex. However, their combination on the same samples in such a long lasting fabrication process entails new difficulties by itself.
Each lithographic fabrication step included the removal of a resist mask in a solvent bath at elevated temperature and the application of ultrasound to clean the surface. This always included the risk of sample destruction due to soaking of the PDMS with solvent or delamination. However, avoiding baths in acetone – leading to pronounced swelling of PDMS [180] – prevented problems due to the PDMS used for the embedding. Also every additional layer of parylene (between the two layers of conducting tracks and on top of the second layer of conducting tracks) enclosed the complete sample and made it less sensitive to the fabrication steps including baths in liquids. However, the fabricated VIAs opened paths into the parylene stack on top of the device. Also bad adhesion of the parylene became problematic. While adhesion of the used resist masks and the adhesion of the aluminum hard mask was good enough for the structuring processes the adhesion of the different parylene layers on each other was hardly satisfactory. While the adhesion was sufficient during most of the fabrication process it started to show signs of delamination during the fabrication of the 3rd VIA layer. After the deposition of the aluminum for the hardmask, it could be observed on several samples that the parylene layers did no longer adhere on their complete surface, but that blisters formed. It was however not possible to see where exactly (between which layers) delamination occurred.
It is obvious that the risk of manufacturing defects increases with the number of fabrication steps. Depending on where in the process these manufacturing defects occur they can affect following steps. However, during the fabrication of the demonstrator system no manufacturing defects occurred that did not allow further processing of the samples.
The completed system was not detached from its rigid glass handle substrate and looked as expected from the layout (Fig. 4.31).

The handle substrate is $49\,\text{mm} \times 49\,\text{mm}$ in size, but the structures of the demonstrator system span only an area of approximately $35\,\text{mm} \times 35\,\text{mm}$. At the edges of the substrate there is an approximately $1\,\text{mm}$ wide frame where the sample is covered by the unstructured metalizations of the two layers of conducting tracks (see Fig. 4.31 left). They originate from the edges of the samples masked by tape during etching of the conducting tracks to prevent unwanted etching of PDMS, because edges of the samples often showed defects. While all tracks made of Ti/Au/Ti look dark grey due to the titanium (Fig. 4.31 right) the contact pads and electrodes

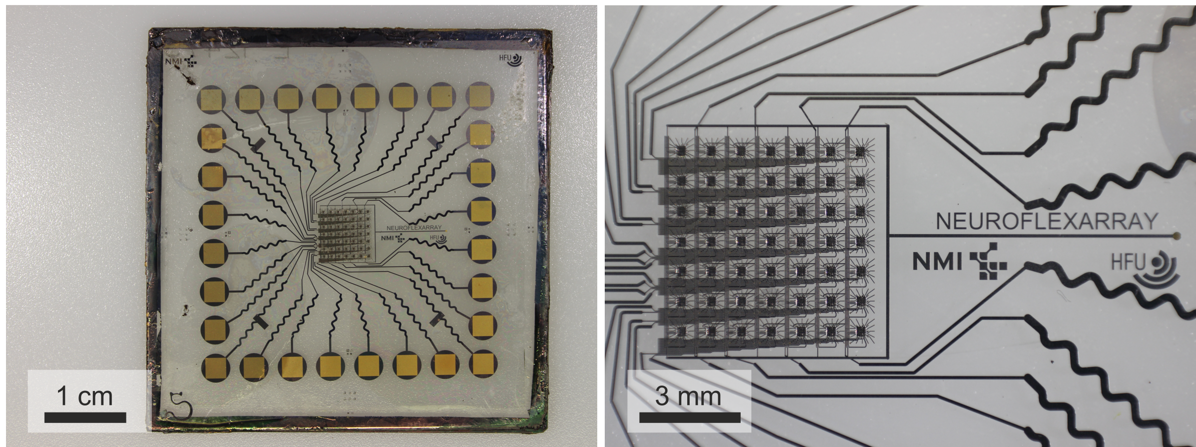


Figure 4.31: Pictures of the completed demonstrator system. Left: The complete sample on a $49\,\text{mm} \times 49\,\text{mm}$ glass handle substrate. Right: Picture of the central part of the system with the die array and the electrode array, respectively.

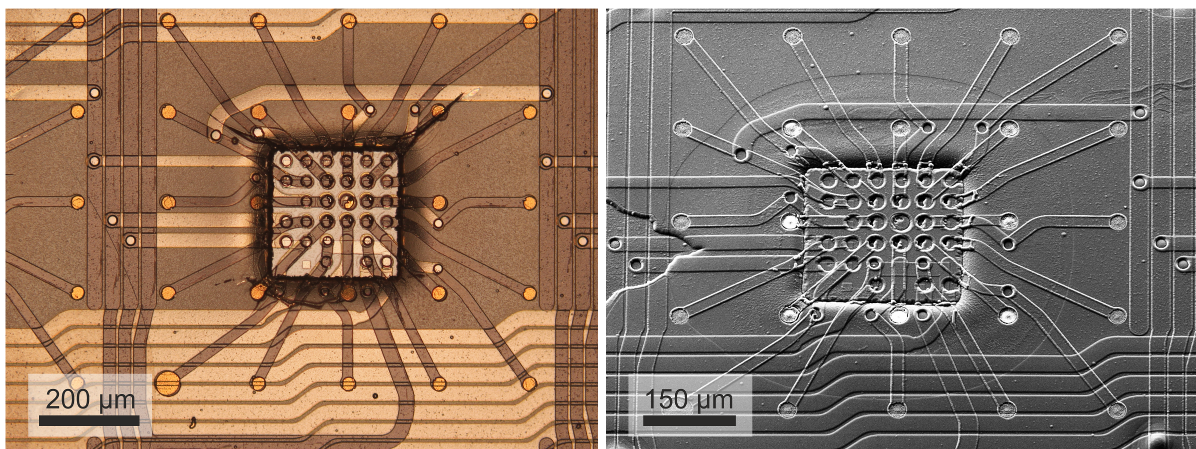


Figure 4.32: Pictures showing each one cluster of a completed demonstrator system. Left: Light microscope picture showing both layers of conducting tracks. Around the die-dummy the fabricated tracks are disturbed. Right: SEM-picture taken under an angle of $30°$. The surface shows unwanted topography from different fabrication steps.

appear golden (Fig. 4.31 left and Fig. 4.32 left), because the top titanium was etched away after etching of the 3rd VIA layer exposing the gold.
The resolution of the photolithographic processes was sufficient to structure all tracks properly (Fig. 4.32), except for those positions where the surface topography was too high (see section 4.3.2).
While the fabrication of the VIAs using an aluminum hardmask worked fine in principle, this step was prone to introduce unwanted surface topography. Often such effects showed around the individual clusters of the array where most of the structures' details concentrated and where there was initial surface topography from the embedding process already affecting the processes (Fig. 4.32 right).

Many fabrication steps were repeated several times. However, changing surface topography and roughness could strongly influence the result. Therefore, the same process on the same sample, e.g. for the etching of VIAs, might work better or worse for the second layer as for the first layer.
While the demonstrator system was completely built, all samples displayed mistakes. While some samples included big mistakes as short circuits or interrupted conducting tracks affecting the complete array, others displayed only minor mistakes affecting only spatially confined parts of the array. Yet, no successful electrical measurement could be performed on any sample proving electrical connection of the die-dummies or giving a hint on the resistance of the tracks and the VIAs.

Chapter 5

Discussion

In this chapter the results presented in the last chapter are discussed.

5.1 transfer and assembly of dies

An important aim of the transfer process is the possibility to efficiently use the wafer area during the fabrication of the dies. If the dies of $(250\,\mu\mathrm{m})^2$ size were fabricated in their final spacing in the array of $900\,\mu\mathrm{m}$, only $\left(\frac{250\,\mu\mathrm{m}}{900\,\mu\mathrm{m}}\right)^2 \approx 8\%$ of the wafer area would have been used. Fabricating them with a spacing of only $50\,\mu\mathrm{m}$ – required for separation by dicing – and increasing the spacing of neighboring dies in an array with the transfer printing process results in an area usage of $\left(\frac{250\,\mu\mathrm{m}}{300\,\mu\mathrm{m}}\right)^2 \approx 70\%$.

5.1.1 measurement of pull-off strength

The aim of the performed measurements was to explore the fundamental feasibility of a transfer printing process based on PDMS stamps picking dies, with an edge length of only $250\,\mu\mathrm{m}$, from a UV-curable dicing tape. Trial of different stamps and different parameters during the measurement of the stamps pull-off strength were conducted to reveal a route towards a reliable process. The required pull-off strength to pick up dies from the exposed tape was performed to provide a reference value on what the pull-off strength of the dies should exceed. It showed that the pull-off strength of the fabricated stamps was comparable to the required pull-off strength and thus the envisioned process was conceivable. A mechanical loosening of the dies on the tape markedly decreases the required strength to pull them off and thus allows a reliable picking process using the PDMS stamps. However, the conducted number of tests was not sufficient to fully characterize the transfer printing process in all details, but in some cases allows only guesses on the nature of the process. Peel-tests with the tape were performed to validate the exposure process by comparing the obtained values to those provided by the manufacturer.
The value for the adhesion of the UV-tape obtained in the peel-test was in relatively good agreement with the value given in the datasheet provided by the manufacturer. The exposed UV-tape peeled off in a wide bow and thus the measurements were not in accordance with

DIN EN 1939:2003-12 method 1. Still, the obtained value is in good agreement with the one provided by the manufacturer and thus the exposure was sufficient. However, the used dose for exposure was more than 150 times higher than recommended in the datasheet. In order to obtain the recommended dosage an exposure time of few seconds, in strong contrast to the 13 min used, should have been enough. For this discrepancy no satisfying explanation can be given.
The resolution of the molds used for the casting of the stamps was not as high as the resolution of a SU-8 mold fabricated using photolithography. Thus, the rim of the bumps of the stamps was not perfect. This might also be one origin for the lower pull-off strength of some stamps in comparison to other stamps of the same design and PDMS. Another source of the variance might be surface contamination during measurement.
Not enough repetitions of the measurements with one stamp have been made to demonstrate a decreasing pull-off strength for repeated usage of a stamp. Also it is not clear if the observed small decrease is a temporal effect that would not appear if the stamp was given more time to relax between the repeated measurements or due to permanent alteration.
The three different stamp designs differ in their circumference to area ratio. For the stamps with the small square bumps (22×22 array of square bumps with an edge length of $300\,\mu\mathrm{m}$ each) the total area is $22 \cdot 22 \cdot 0.09\,\mathrm{mm}^2 \approx 43.6\,\mathrm{mm}^2$ and the total circumference of all bumps is $22 \cdot 22 \cdot 4 \cdot 0.3\,\mathrm{mm} \approx 5.8\,\mathrm{m}$. Thus the ratio is $\approx 1.15 \cdot 10^5/\mathrm{m}$. For the stamps with the circular bumps (22×22 array of circular bumps with a diameter of $350\,\mu\mathrm{m}$ each) the ratio is $\approx 1.13 \cdot 10^5/\mathrm{m}$. The circumference of the bumps of the stamps with the design with big square bumps (5×8 array of square bumps with an edge length of 1 mm each) is only 0.16 m and thus the ratio is only $4 \cdot 10^3/\mathrm{m}$.
The fact that there was no significant difference in pull-off strength between the stamps of different designs made of the standard PDMS, but there was a significant difference for the stamps made of the soft PDMS, is a hint that the imperfect rim of the bumps makes a bigger impact in the case of the soft PDMS.
Pull-off strengths in the range of 25 kPa for the stamps made of the standard PDMS are in relatively good agreement with the values of 30 kPa for flat PDMS obtained from Paretkar et al. [127].
The measured required strength, to pull off silicon wafer pieces from the exposed UV-tape, of 61 ± 7 kPa was above the pull-off strength measured for the stamps made of the standard PDMS at a separation speed of 0.6 mm/min. However, for higher separation speeds and the stamps made of the soft PDMS, the obtained values for the pull-off strength were in the range of the measured required pull-off strength and in some cases exceeded it (maximum value measured 121 kPa), hence implying feasibility of the suggested pull-off of the dies from the tape using a PDMS-stamp.
For a reliable process however, the pull-off strength of the stamps should be markedly higher than the required strength. The experiments showed, that the required pull-off strength can be substantially decreased by loosening the wafer pieces after exposure of the tape. A separation speed of 0.6 mm/min $= 10\,\mu\mathrm{m/s}$ used for most of the measurements is rather slow and thus in a real transfer printing process the occurring pull-off strengths of the stamps would probably be higher.

The pull-off strength of the stamps is independent of the size of the elements to be removed. The stamps attach to the whole top surface of the dies, as does the tape, they are attached to, to their whole bottom surface. In comparison, a vacuum nozzle requires a finite area for sealing, and thus the effective area where a force is acting is always smaller than the devices top surface. For decreasing device size the share of the surface area required for sealing increases and thus the maximum pulling force per surface area of the tool decreases.
For example the force required to pull off a die with an edge length of $250\,\mu m$ from the exposed tape would be $61\,\text{kPa} \cdot (250\,\mu\text{m})^2 \approx 3.8\,\text{mN}$. A vacuum tool working with a pressure difference of $91\,\text{kPa}$, requiring a $50\,\mu m$ frame for sealing, can pull on the die with a force of $91\,\text{kPa} \cdot (150\,\mu\text{m})^2 \approx 2\,\text{mN}$. The PDMS stamps at the same time can apply pulling forces of 2 to 4 mN (stamps made of standard PDMS) respectively 2.2 to 4.9 mN (stamps made of soft PDMS).

5.1.2 transfer printing

The transfer printing process was performed using stamps made of the standard PDMS, transferring 7×7 arrays of die-dummies from the exposed UV-tape to sugar coated substrates. The success of the process must be assessed due to three criteria:

- yield: ratio of the array's elements that is transferred
- selectivity: number of elements not belonging to the array that are erroneously transferred
- accuracy: divergence of the elements from their ideal position after the transfer

A high yield and good selectivity were achieved and the accuracy was within reasonable limits. A reliable high yield was achieved when the die-dummies were loosened after exposure of the tape and prior to the transfer printing procedure. This matches with the results obtained from the measurements discussed in the last section. While a yield of 100% was only reached in individual cases an average yield of more than 90% is a satisfying result.
Selectivity in general was very good. Bad selectivity – when also wrong elements were transferred – would either reduce the effective yield of following transfer printing procedures, as some elements were already falsely transferred in the previous process and are thus missing. Or it would reduce the number of transfer printing processes that can be conducted, as less complete arrays can be picked from the sample, and thus dies would be wasted. However, an array containing additional elements can still be processed and does not affect the overall fabrication process. The PDMS-stamps were usually fabricated with a profile depth of $100\,\mu m$. The complete area of the stamp was covered by a thin PDMS film. However, this film originated from the liquid PDMS creeping between the mold and the glass pressed on top, building the backbone of the stamp. Therefore, this film was very thin compared to the profile depth. A load of 3 N applied to the stamp, when the stamp is pressed onto the die-dummies, leads to a pressure of $\frac{3\,\text{N}}{7 \cdot 7 \cdot (250\,\mu\text{m})^2} \approx 0.98\,\text{MPa}$. Depending on the Young's modulus of the used PDMS the profile is either compressed to approximately half its thickness (standard PDMS $E \approx 1.32\,\text{MPa}$) or flattened (soft PDMS $E \approx 0.32\,\text{MPa}$). This explains the lower selectivity for the stamps made

of the soft PDMS.
The accuracy of the array's elements could be affected at various steps during the process. The loss of order during drying after dicing and prior to the transfer printing process that was in some cases observed (Fig. 4.4), is a well known problem in microstructure fabrication [181]. Due to the high surface tension of water the samples cannot be completely dried by blowing with nitrogen. If the remaining water is unevenly distributed in the saw kerfs between the separated dies, capillary forces occur and disturb the order when the water evaporates slowly. The acting forces depend on the surface tension of the water, which at 20°C is $\gamma = 72.75$ mN/m increasing with decreasing temperature. For the geometry of the dies separated within this work (250 μm width, 200 μm height, 60 μm kerf width) the force working on the side of one die can be calculated to be approximately 60 μN [182, 183]. Shear tests on the used dicing tape with $2\,\text{mm} \times 2\,\text{mm}$ sized wafer pieces were performed to obtain comparables to the expected value for the working capillary force. The measured values must be divided by a factor of 64 to gain the forces holding the dies on the tape. Depending on the shear speed the maximum forces correspond to ≈ 200 mN (500 μm/s), ≈ 130 mN (100 μm/s) respectively ≈ 30 mN (10 μm/s) and are thus about three orders of magnitude larger than the capillary forces. However, once the wafer pieces were set in motion the force decreased to values of few mN (shear speed of 10 μm/s) being sufficient to displace the wafer pieces on the tape. When for complete separation of the wafer also the tape is partly cut by the blade the effective area exposed to the water film increases further, as the depth of the cut tape adds to the height of the wafer pieces. Still, based on the measured forces a loss of order due to drying is unexpected and further other mechanisms might be involved.
In order to prevent disturbances due to drying effects the surface tension of the fluid in the trenches should be reduced. Heating or replacement of the water with methanol having a surface tension of only 22.60 mN/m are two commonly applied possibilities [181, 183]. The additions of surfactants is another possibility to lower surface tension. It is however important that the applied drying process does not lead to any surface contamination of the dies for example by solvating glue from the dicing tape.
The transfer printing process itself also led to a lower accuracy compared to the initial situation on the wafer, however the introduced changes were much smaller, than those that could occur due to uneven drying after dicing. The accuracy of the relative positions of the elements of one array after the transfer printing was sufficient for most elements, although it was not perfect and the inaccuracies usually were only marginally smaller than the maximum tolerable displacement of 20 μm. Frequently few die-dummies of an array were misplaced by more than 20 μm or rotated.
The judgment of the accuracy based on the superimposing of microscope pictures does not allow the fast and exact examination of many arrays. The magnification of the microscope should be as high as possible, however has to be chosen in a way that the complete array is photographed at once. The examination of the pictures on a pixel wise scale is only valid, if the optics of the microscope and the camera are perfect and do not introduce any distortion. While the array covers an array of several millimeters, the position of the arrays elements has to be determined to within a few micrometers. This corresponds to a factor > 1000 between the size of the image and the size of the distances of interest. The performed superimposing with a contrast inverted

rotated copy, or a drawn model array highlights deviations of the arrays elements from their ideal positions. While the first method gives a fast impression of the deviations (the contact pads on the die-dummies with a size of $15\ \mu m \times 15\ \mu m$ provide a convenient scale), the second method allows an exact quantification of the deviation by counting pixels. Yet, the placement of the drawn ideal model array on top of the picture is done by eye and thus defective. The best control of the accuracy is thus the alignment of a photomask during the fabrication of the electrical connections setting also the accuracy requirements.
At the end the occurring inaccuracies lead to a decreased effective yield of how many elements were transferred in a way making them accessible to the overall fabrication process. Assuming, that the yield of the transfer printing is above 90% and that up to 10% of the die-dummies of an transferred array are inaccessible due to misplacement the effective total yield of the process is approximately 80% and thus from the 49 die-dummies of one 7×7 array usually at least 39 die-dummies of the array should be accessible. Small deviations of the die-dummies from their ideal position below $10\ \mu m$ occurring frequently for most of the die-dummies of an array inhibit perfect alignment of a photomask on the array during the fabrication of the electrical connections. However, the aim of the process was never to allow perfect alignment but to enable electrical connection of as many of the dies of one array as possible. This is also possible with only partial overlap between contact pad and VIA/conducting track.

5.2 embedding of dies

The aim of the embedding process was to level the topography due to the dies height providing a flat surface between the dies and the surrounding material, thus enabling the use of thin film fabrication processes and photolithography. This goal was in principle fulfilled, although standard processes for the fabrication of the electrical connections might not be applicable. The fabrication of the electrical connections was the next step in the overall fabrication process of the envisioned device. It was conducted on the same samples discussed in this section and thus proves their surface to be feasible for the use of thin film fabrication processes and photolithography, although the successful fabrication required the development of specific processes as discussed in the next section.
The shellac film used within the developed process used to be a useful and practical choice as a sacrificial layer. Softening by heating it up also allowed its use as a receiving substrate during the transfer step performed to flip the array. The preparation of the shellac film however, can be further improved. A thinner shellac layer below $5\ \mu m$ thickness has shown to be sufficient as a sacrificial layer and would reduce the maximum amplitude by which the dies protrude from the surface. An optimized process and thinner layer thickness also enables the possibility to reduce the waviness of the shellac film's surface. However, no statement can be made on how the surface of the shellac film looks when the film is heated up or solvated with ethanol during the aforementioned turning step, when the surface of the film matters most.
This turning step has the greatest influence on the resulting surface topography of the embedding process. The temperature based process heating the shellac up in order to liquefy the shellac film however seems to be a good and reliable process. Within this work the temperature for

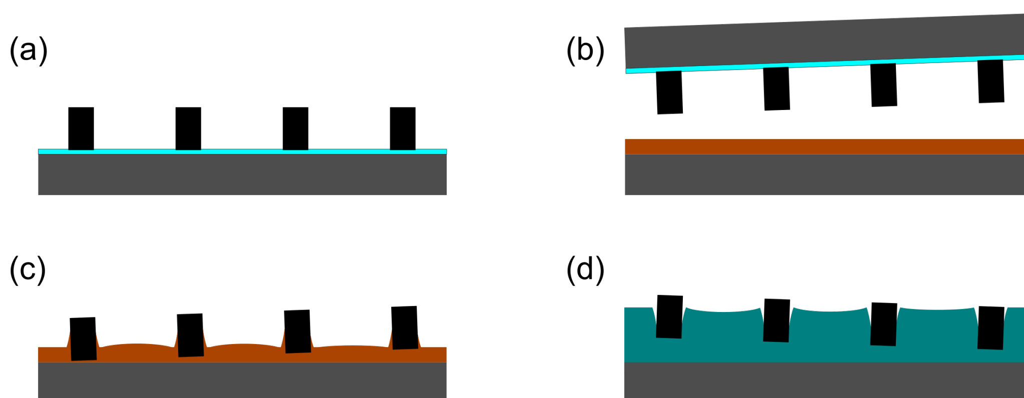


Figure 5.1: Schematic showing how the turning step prior to the embedding affects the resulting surface topography after embedding. (a) Array sitting on a sugar coated substrate. (b) The array is brought to contact to the shellac coated substrate. No mechanism preventing tilt is implemented and thus parallel contact of both substrates is not assured. (c) Adhesion to the shellac film is achieved by softening the shellac either by temperature or by solvating it with ethanol. Surface tension of the liquefied shellac leads to the formation of menisci around the individual elements of the array. Material displacement from the elements can further change the former flat surface of the shellac film. Any tilt in (b) results in the elements being pushed differently deep into the shellac. (d) The embedding process perfectly molds the interface between the shellac and the elements of the array or the air (between the elements of the array), respectively. Thus, the shellac menisci fixating the elements result in trenches around the elements.

this step was only changed in steps of 10°C. While a temperature of 80°C proved to be too low to result in a reliable transfer, a temperature of 90°C or 100°C proved to be suitable. For temperatures above 100°C the resulting surface topography showed high amplitudes. So, a screening of the temperatures between 80°C and 100°C in smaller temperature steps might result in an even better temperature choice, providing high reliability at minimum amplitude of the resulting surface topography.
The pouring in PDMS worked fine and can easily be performed with several samples in parallel. The process can be applied to dies of arbitrary thickness by adapting the thickness of the used spacers. As silicone can affect adhesion negatively all process steps with the uncured PDMS should be conducted in a separate clean room, to prevent any contamination disturbing other processes performed in the clean room.
The resulting surface topography at the end of the embedding process is a replica of the interface between the shellac and the elements of the array or – between the elements of the array – the shellac and the air, respectively. Hence, it is obvious why the turning step affects the resulting surface topography so much. The parylene deposition prior to the pouring of the PDMS scarcely affects the topography, because the deposited layer was thin and the parylene deposition process is conformal. Figure 5.1 sketches the process steps forming the surface topography.

At the beginning of the process the array is attached to a sugar film. Any formation of a meniscus at the dies or unevenness of the sugar surface does not affect the process (Fig. 5.1 (a)). In the turning process the substrate with sugar coating and with the array attached is brought to contact with a shellac coated substrate (Fig. 5.1 (b)). Two procedures have been tried. When

the array was actively brought to contact with the shellac film and pressed in with the fineplacer plane-parallel contact could not be assured. This then resulted in the dies at one side of the array being pressed deep inside the shellac, while the dies at the other side of the array hardly came into contact with the shellac. Thus, in this process step the loss of part of the arrays' elements frequently occurred. In the second procedure used, the array was dropped into the shellac from approximately 1 mm above the shellac. This led to a more plane-parallel contact. After the sugar is dissolved with water the array is only attached to the shellac film. Where the dies are pressed into the shellac, material is displaced. The surface tension of the softened or solvated shellac leads to the formation of menisci at the edges of the dies (Fig. 5.1 (c)). These menisci embrace the dies and thus fixate them to the substrate. The lower the viscosity of the shellac at its surface (either due to heating or solvating) the more pronounced is the formation of this meniscus. The following steps then mold this surface (Fig. 5.1 (d)).
Compared to the embedding process developed by Barz et al. [70] the embedding process differs in several points, although both processes use shellac. While the process in this work uses shellac as sacrificial layer and as "sticky layer" in a transfer process, the process of Barz et al. uses the shellac as temporary filling material to level the topography. In contrast the process in this work uses PDMS for the leveling which remains in the sample, building a foil of homogeneous thickness. The resulting surface topography in the embedding process of Barz et al. should be perfectly flat. The resulting surface in their process is molded by the shellac. The dies sit on a planar dry PDMS surface, held by van der Waals forces. Thus, the surface molded by the shellac is the flat interface between the PDMS and the dies or air, which is the surface of the PDMS. In the process of this work, the dies are held by the shellac film, which was liquid when it came into contact with the dies, leading to the molding of a different – not perfectly flat surface – as discussed above. The advantage of the process developed in this work is that is can not only be applied to ultra-thin dies, but is unaffected by the dies-height, because the PDMS can be cast thicker than the shellac.
The use of the two component PDMS for the embedding is beneficial, because it does not outgas during curing allowing also thick layers. Processing is performed at low temperature, but the PDMS also limits the maximum temperature of following process steps. Thus, polyimide cannot be used on top of the embedded array, because it would require baking at $\approx 350°$C. So parylene C has to be used as insulating material layer between the different layers of conducting tracks.

5.3 fabrication of electrical connections

The fabrication of the electrical connections is the last step in the overall fabrication process developed within this work, and the assembly and embedding process (discussed in chapters 5.1 and 5.2) have been developed to enable this last fabrication step.
The relative positions of the individual dies of an array were accurate enough to allow reasonable alignment of a photomask on the array. As expected, perfect alignment of the masks structures on all dies of an array was not possible. But, for most dies of an array sufficient overlap between the structures was possible confirming the results concerning accuracy of

chapter 4.1.
The surfaces of the embedded arrays were smooth enough to allow the spin coating of thin resist films, covering little surface topography.

5.3.1 fabrication of VIAs

Three different processes have been proposed for the fabrication of the VIAs (Fig. 3.10). It has been shown that due to the formation of cracks in the surface the processes where the VIAs are etched against a resist mask are not applicable (processes (a) and (c) in Fig. 3.10). Hence, the only remaining applicable process is the one based on a hardmask (process (b) in Fig. 3.10). For the success of this process the choice of a suitable material for the hardmask is essential. The flanks of the VIAs should not be vertical, but sloped to facilitate an easy overcoming of the vertical distance between the two layers of conducting tracks. While the proposed processes differ in the options to obtain sloped flanks the process was not optimized to result in optimal flank angles in this work.
The process based on a positive tone resist and a dark field mask would only have been applicable for the fabrication of the second and third layer. However, the process is most suited to fabricate good flank angles of the VIAs, because the positive tone resist mask can feature an overcut that then during etching is transferred to the parylene resulting in sloped flanks. The other processes can only produce flat flank angles through isotropic etching and thus require a set of proper etching parameters. The etching parameters used in this work resulted in steep flank angles, for a better result the etching parameters should be varied and the resulting flank angles determined e.g. using a FIB milling (focused ion beam) in combination with SEM imaging.
For the processes in which the VIAs are etched against a resist mask it has definitely been shown that the cracks in the resist form during evacuation prior to etching and not during etching. Thus, the crack forming mechanism is expected to be based on expansion of the PDMS – cured under atmospheric pressure – in vacuum. The parylene covering the PDMS was deposited in vacuum, thus the parylene was deposited on top of the expanded PDMS and thus does not tear in vacuum, when the PDMS expands again. The resist however is coated onto the sample at atmospheric pressure and thus can not resist the stresses when the PDMS expands in the vacuum and the surface it was deposited on stretches and moves.
So the use of a hardmask is the only remaining process for the fabrication of the VIAs. Yet, the choice of the hardmask material is crucial to the process. Low internal stress – preventing the formation of cracks – and easy wet etch are essential.
In this work chromium and aluminum were investigated as hardmask. The chromium caused the formation of numerous cracks in the surface due to internal stress and is thus unsuitable. Aluminum caused no cracks and was easy to wet etch, meaning the etching solution was selective and not extremely toxic (as for example HF would have been). Still aluminum is possibly not the optimal material for the hardmask, as it causes problems when it is removed after the etching of the VIAs. The etching solution can then attack the material under the newly etched VIAs. The first layer of VIAs connects the first layer of conducting tracks to the dies and thus the material at the bottom of the VIAs is that of the dies' contact pads. The following

layers of VIAs are etched towards the two layers of conducting tracks and thus the material at the bottom of the VIAs is the Ti/Au/Ti of the conducting tracks. To overcome the problem of possible accidental etching of contact sites, in this work die-dummies with the contact sites made of chromium were used. For real CMOS dies where the material of the contact sites cannot be chosen arbitrarily a possibility to prevent problems would be to cover the contact pads with a protecting layer structured on top prior to the start of the process developed within this work.

5.3.2 fabrication of conducting tracks

The metalization structured for the conducting tracks also covered small vertical areas and thus the tracks can pass small topography as the edge of the embedded dies when the dies protruded from the surface by several micrometres. It was however also shown that for too big height differences tracks tend to be interrupted at an edge where they have to follow a 90° bend from the horizontal to the vertical. Also, layer thickness on areas with a vertical component will be smaller and thus weak points will form.
The observed formation of a halo like unstructured gold film around the dies was attributed to a resulting change in resist thickness, although the resist at least partially followed surface topography. As a consequence exposure was not sufficient to reach the bottom of the thicker resist layer, leaving the resist layer unexposed at its bottom. As a positive tone resist was used the unexposed resist was not dissolved during development and thus the complete metalization was covered by resist during etching, preventing its structuring in these areas (Fig. 4.19). To achieve exposure of the resist on its full thickness longer exposure times have been tried. It was shown however that the differences between different samples – using the same exposure times – were greater than those resulting from a doubling of the exposure time. A too long exposure at the same time results in insufficient resolution of the process. This then implies that no reliable exposure time being optimal for all samples can be found. So, to obtain better results using this process it is inevitable to improve the surface topography after embedding.
Yet, alternative processes that could handle the topography are available. Using a thicker resist could lower the relative thickness inhomogeneity and thus make the resist less sensitive with regard to the exposure dose. Furthermore, the negative resist used for the fabrication of the VIAs seemed not to be affected by the surface topography and thus a lift-off process using a negative resist seems feasible for the structuring of the conducting tracks. However, a lift-off process is challenging and requires extensive process development too. Other methods for the deposition of the resist besides spin coating – e.g. spray coating – could provide homogeneous resist thicknesses on surfaces containing topography.

5.4 mechanical properties of the foil-system

In order to achieve a stable flexible electrically active implant consideration of the mechanical properties of the device is essential. Bending of a flexible foil-system is accompanied by stretching and compression of different parts of the system, which can cause failure of less

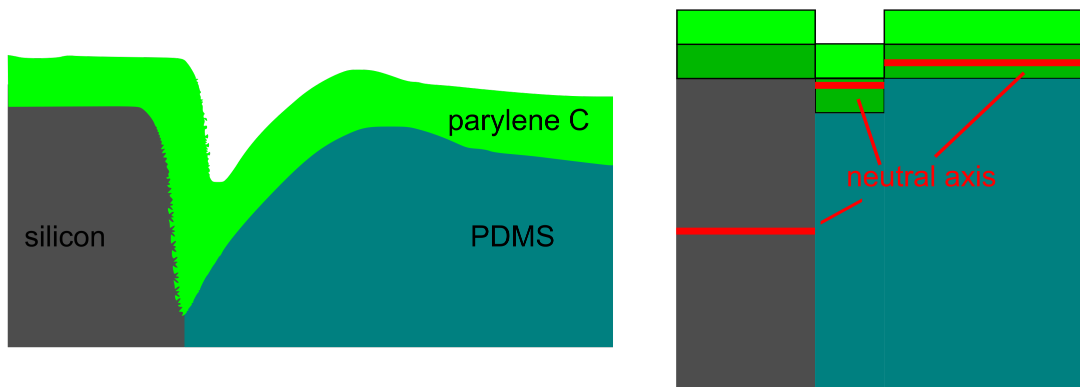


Figure 5.2: Left: Sketch of material distribution near the edge of an embedded die. The topography is formed by the die (silicon) and the PDMS and is conformally coated by the parylene C. Around the die the surface builds a trench, where thus the thickness of the PDMS is less. Right: Sketch simplifying the material distribution near the edge of an embedded die. Three different sections are shown. In the left section there is the silicon die covered by several layers of parylene. The neutral axis is somewhere near the center of the die. In the right section the same space filled by the silicon die in the left section is filled by PDMS. Due to the lower Young's modulus the neutral axis is in the middle of the parylene layers on top, only slightly shifted towards the PDMS. In the middle section in between the total thickness is less due to the trench around the die. Compared to the right section the neutral axis is slightly shifted away from the PDMS towards the center of the parylene layers.

stretchable – probably brittle – components of the device. Thus, the location of the neutral axis within the system is of vital interest. Besides that, weak points arising in combination with a wet environment have to be identified. One such weak point is insufficient adhesion between the individual layers of the system, another is the existence of paths for water intrusion into the system. These weak points are also discussed in this section.

Calculation of the neutral axis for different parylene/PDMS stacks showed that, although the PDMS is more than ten times thicker than the parylene, the parylene mostly determines the mechanical properties of the system. The relevant parameter is the product $E \cdot d$ of Young's modulus and layer thickness, but the Young's moduli of the different materials within the system differ by several orders of magnitude. Thus, during an applied load the foil-system is scarcely stretched at the positions of the dies.

The different systems (material stacks) presented in Table 4.1 are all very close to the device that is fabricated, or rather different parts of a fabricated system. A thickness of the parylene C of $12\,\mu\mathrm{m}$ for example corresponds to four layers with $3\,\mu\mathrm{m}$ thickness each (1 layer prior to PDMS pouring, 1 layer on top of the embedded dies, 1 layer between the to layers of conducting tracks, 1 layer on top of the upper layer of conducting tracks) as they are deposited in the fabrication process. PDMS thicknesses of $210\,\mu\mathrm{m}$ and $525\,\mu\mathrm{m}$ correspond to the spacers mostly used within this work.

That the neutral axis of the system is not near the geometrical center of the stack, but within the top parylene layer is beneficial because it results in the strain during bending being less in the relevant parylene layer on top including all sensitive conducting tracks etc., while the strain on the opposing PDMS surface holding no sensitive structures is increased.

However, with regard to the real device the modeling of the device as a stack of homogeneous

thickness with alternating regions of silicon/parylene and PDMS/parylene is not valid. As shown in section 4.2 the surface of the device includes topography especially near the edges of the embedded dies. The surface topography is determined by the silicon and the PDMS, while the parylene C just coats the surface without changing topography (Fig. 5.2 left). Conducting tracks – considered as stress sensitive source of failure, not affecting the mechanical properties of the system – are deposited onto the parylene, which is composed of different layers. Therefore, the tracks follow the surface topography. With increasing distance from the neutral axis strain during bending increases. On top of the die the tracks are far away from the neutral axis (Fig. 5.2 right), however due to the high Young's modulus of the silicon die the region of the die faces almost no bending. Besides the die, where there is PDMS under the parylene, the neutral axis is near the center of the parylene, slightly shifted towards the PDMS (Fig. 5.2 right). Directly after the edge of the die the surface forms a trench with decreased thickness of the PDMS, thus the neutral axis is less shifted towards the PDMS. This means that the distance of a conducting track, following the surface topography, from the neutral axis changes. As a result the track can – in principle – pass regions without strain, regions with tensile strain, and regions with compressive strain. For a change from a $210\,\mu\mathrm{m}$ thick to a $190\,\mu\mathrm{m}$ thick PDMS layer the neutral axis shifts by only $0.16\,\mu\mathrm{m}$ ("system 1" and "system 4" in Tab. 4.1) which is less than the thickness of the tracks. The calculated difference in strain near the surface is below 0.05% and thus the effect might be negligible.

The surface topography can also affect the effective parylene thickness. For non-horizontal areas the vertical thickness of the parylene with a thickness d_0 vertical to the surface is $d_{\text{eff}} = \frac{1}{\cos(\alpha)} \cdot d_0$. For an angle of $30°$ layer thickness increases by $\approx 15\%$. This corresponds to the difference between "system 1" and "system 3" in Tab. 4.1 with the neutral axis shifted by $0.88\,\mu\mathrm{m}$ with respect to the surface.

So in summary the surface topography can lead to an imbalanced strain along the conducting tracks that can result in predetermined breaking points. Still, the effects are very small and thus other effects not considered here might have a bigger impact.

The location of the neutral axis is – as mentioned above – primarily determined by the thickness of the parylene C. Its position in principle can be set by changing the thickness of the PDMS and the parylene. For a PDMS thickness of $525\,\mu\mathrm{m}$ ("system 2" in Tab. 4.1) the neutral axis is almost at the interface between PDMS and parylene. The thickness of the parylene is composed of the thicknesses of four individual layers. The upper three layers are the insulating layers between the conducting tracks and the environment and thus part of the electrically active system. VIAs are etched through these layers, and thus their thickness is important. It should not be too thin, in order to allow good electrical insulation between the different layers of conducting tracks, but should also not be too thick. The fourth layer however, the one directly at the interface with the PDMS, can be chosen more freely as it does not have to be structured and is not important for the electrical insulation. Therefore, it can be used to set the location of the neutral axis.

Due to their high Young's modulus ultra-thin barrier layers can already strongly affect the system. An Al_2O_3 layer of only $20\,\mathrm{nm}$ thickness between the PDMS and the parylene can already shift the neutral axis by $0.53\,\mu\mathrm{m}$ ("system 8" in Tab. 4.1). This strong influence of a thin barrier layer on the mechanical properties of a parylene foil was also observed in

experiment [177]. In a symmetrical stack with a second barrier layer at the top the shift would of course be less. Considering the fragility of the Al_2O_3 or other brittle films that could be used as a water vapor barrier, they should be located as close to the neutral axis as possible, enclosing all parts of the system that are sensitive to the intrusion of water.
With regard to this possibility to engineer the location of the neutral axis within the foil-system, the question of its ideal position arises. As there are two layers of conducting tracks, there is no obvious position. Hence, a position between both layer of conducting tracks seems favorable. For a thickness of the upper three parylene layers of $3\ \mu m$ each this would be $4.5\ \mu m$ under the top surface. To achieve this the PDMS thickness should be as small as possible (limited by the thickness of the dies) and the lowest (fourth) parylene layer should also be very thin. A barrier layer on top could further shift the neutral axis towards the surface (compare “system 9” in Tab. 4.1). However, protection with an additional parylene C layer or an atomic layer deposited barrier seems more relevant to the other side with the highly permeable PDMS.
Furthermore, an exact engineering of the location of the neutral axis would require consideration of internal stresses of the different layers.

Considering failure not due to bending, but due to the harsh humid environment of an implant in the body the locations prone to water intrusion are of most interest. ALD layers are considered as barrier layers. They should confine the dies as well as all conducting tracks as they are most sensitive to water induced failure. As discussed above barrier layers should also be located as close as possible to the neutral axis, as they are brittle and the formation of cracks within the layer makes it obsolete. Further, their integration into the fabrication process can cause difficulties. Despite their small thickness they have to be considered as a separate layer within the system. This holds especially for cases where the layer has to be structured because it interrupts electrical conduction. The most promising possibility to integrate ALD barrier layers into the fabrication process is thus to deposit one barrier layer onto the parylene prior to the pouring of the PDMS. This barrier hinders water intrusion from the backside and does not have to be structured at all. A second ALD layer should then be deposited on the surface at the end hindering water intrusion from the front side. This ALD layer would cover all electrodes and thus needs to be structured.
Furthermore, besides water intrusion due to diffusion through the polymeric layers, the system contains another weak point at its ends. While the considerations above have been made for an infinite layer stack the fabricated device covers an area of only several cm^2 and at its ends the cross section of the different layers is openly exposed. During fabrication the system is attached to a handle substrate and the conformal deposition process of the parylene covers the complete substrate including its backside and thus during fabrication the system includes no open ends. However, to detach the complete device from this handle substrate at the end, its contour has to be cut out resulting then in an open rim. This is a crucial weak point for water intrusion that is also not aided by the addition of barrier layers. The only possibility to prevent this open rim would be to detach the device directly after the structuring of the second layer of conducting tracks so that the final parylene layers covers the complete device including the rim and the backside. However, this is then problematic for the last structuring step opening this parylene layer on top of the electrodes.

The last aspect to be considered to obtain a stable device is adhesion between the different layers of the system. This is a critical issue for parylene. Due to the room temperature deposition process the different parylene layers do not connect to form a single continuous layer, as it is possible for other polymeric foils. Good adhesion can only be achieved by proper pretreatment (e.g. using different plasmas) and the use of adhesion promoting agents.

5.5 characterization of ALD layers

Thin films were deposited using ALD and characterized exploiting their use in a flexible electrically active implant. Possible applications of the examined layers in such devices could be barriers against water vapor intrusion, adhesion promotion and electrical insulation.
While good adhesion is essential in order to obtain a longtime stable flexible implant it was not an object of investigation within this work. Thus, no statement on the ability of ALD coatings to facilitate good adhesion can be given. The electrical properties of Al_2O_3 and TiO_2 layers deposited using ALD were examined and are discussed in the following section. The most promising application of ALD layers in a flexible electrically active implant is their use as barriers. The permeability of ALD coated foils was thus investigated and the results obtained confirm the expected substantial potential of ALD coatings as gas diffusion barriers. All ALD films investigated were successfully deposited at temperatures $\leq 120°$C, which is a precondition for their combination with polymers in a flexible device.

5.5.1 electrical characterization

The electrical properties of Al_2O_3, TiO_2 and Al_2O_3/TiO_2 multilayer films deposited with plasma-enhanced ALD at temperatures $\leq 120°$C were examined. The prepared samples exhibited measurement fields of $1\,mm^2$, $2\,mm^2$ and $4\,mm^2$ size. Despite these large measurement fields no effect of defects as for example pinholes was recognized. The Al_2O_3 films provide good electrical insulation with high resistances and low leakage currents below $4 \cdot 10^{-3}$ nA/mm^2 for an applied voltage of $2\,$V even for layers as thin as $23\,$nm. The dielectric strength of the films was $\approx 7\,$MV/cm. The TiO_2 films in contrast revealed semiconductor behavior during the performed leakage current measurements and are thus not suitable for electrical insulation. Still they are important for possible applications in an implant due to their reported high chemical stability. The combination of both materials in multilayers ($100\,$nm thick) resulted in layers that could withstand voltages above $40\,$V before electrical breakdown occurred.
The chosen sample layout allowed reliable measurements and the impedance measurements on the measurement fields with different areas (and different area to circumference ratios) resulted in the expected area dependency. Thus, there are no relevant edge effects. The chosen protocols for the leakage current measurements were chosen based on the measured current over time measurements after an applied $1\,$V voltage step (Fig. 4.22). For the measurements on the Al_2O_3 films the step duration was set to $240\,$s while the voltage step was only $\frac{1}{20}$ V. Thus, there was sufficient time for any charging currents to decay so that the measured current was the time independent leakage current. While the charging current of a capacitor decays

exponentially following $e^{-t/\tau}$ the observed decay was not exponential within the first minute but was proportional to $\frac{1}{t}$. This unexpected behavior cannot be related to the Al_2O_3, but seems to originate from the measurement unit. For the measurements on the TiO_2 films the step duration was set to 5 s, as there was some decay within the first few seconds, before the current increased linearly with time. The short step duration of 5 seconds thus provided comparable current values for different samples, while longer step duration emphasized the occurring effects related to the increasing current with time.
The obtained values for the permittivity of the Al_2O_3 films (between 8.05 and 10.42) are close to the value of 7.6 found in literature [158], but tend to be slightly higher. This can be understood as a sign for dense films. The values for the leakage current at 2 V are in good agreement to those given in literature. The measured values for the dielectric strength of the films are slightly larger than the 5.2 MV/cm given in literature for a 12 nm thick layer [158].
For the TiO_2 films also the permittivity of the TiO_2 films was calculated using the obtained impedance spectra. For the films deposited in plasma processes at temperatures $\leq 120°C$ the values obtained were in the range between 33.63 and 35.59 which is in good agreement with the literature values reported for anatase TiO_2 that are between 30 and 40 [159]. For the films deposited in a plasma process at 300°C the obtained values for the permittivity were slightly larger (between 44.97 and 58.12). This indicates that these films differ in their crystallinity. The one value obtained for a TiO_2 film deposited in a thermal process at 300°C of 119.58 is in the range reported for rutile structured TiO_2 [159].
The observed linear increase of current with time for an applied constant voltage was unexpected and thus it was attempted to eliminate all possible sources of error e.g. a temperature dependence of the films resistance and heating of the film due to the high current flow. However, any temperature effect could be excluded by actively cooling the sample. Further, any temperature effect would be smaller and also after some time an equilibrium temperature should be reached and thus the resistance change should come to an end.
Two different effects could be observed. The films deposited using different processes showed different behaviors. The films deposited at 100°C and 120°C showed a hysteresis in the measured current-voltage curves (leakage current measurements). Increasing the step length of the individual voltage steps led to wider hysteresis loops. For the films deposited at 300°C strong rectifying behavior was observed i.e. the current-voltage curves were not symmetric for positive and negative voltages. Both effects have been reported in the literature. The TiO_2/metal contact can build a Schottky barrier diode depending on the work-function of the metal [162]. Thus, for further examination of this effect test samples should be fabricated using other metals instead of the used gold. For the application of the TiO_2 films in a flexible electrically active implant the effect is of no relevance, but it is important to keep in mind the non-ohmic behavior and low electrical resistance. The second effect can be associated with the resistive switching behavior reported for TiO_2 films where oxygen vacancies work as dopants [163–165]. Further investigation of the observed hysteresis would thus include analysis of the exact stoichiometry and structure of the deposited TiO_2, as well as more electrical measurements.
The deposited Al_2O_3/TiO_2 multilayer films showed no sign of non-ohmic behavior. This was most likely because the high electrical resistance of the Al_2O_3 overlaid any semiconductor behavior of the TiO_2. From the impedance spectra an effective permittivity $\varepsilon_{\text{effective}}$ (representing

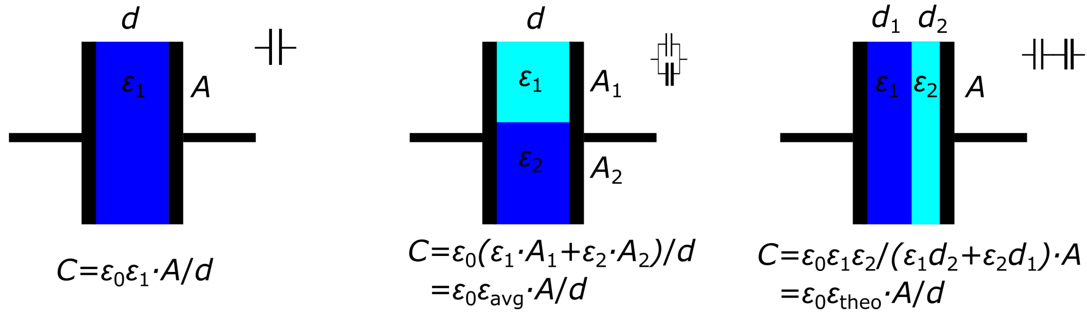


Figure 5.3: Schematic showing the capacitance of different plate capacitors.

the permitivitty of a single material replacing the multilayers while resulting in the same specific capacitance) was calculated for each multilayer. Based on the values obtained for the permittivities of the Al_2O_3 and the TiO_2 and the exact composition of the multilayer (thickness of the individual layers) an expected value for the effective permittivity $\varepsilon_{\text{theo}}$ of the multilayer can be calculated. The capacitance C for a plate capacitor of area A and spacing d between the plates, filled with a material with permittivity ε, is $C = \varepsilon_0 \varepsilon \frac{A}{d}$ with the vacuum permittivity ε_0 (Fig. 5.3 left). The capacitance of a plate capacitor filled with several layers (parallel to its plates) of different materials with different thicknesses d_i and permittivities ε_i is equal to the capacitance of the individual capacitors C_i (plate separation d_i, permittivity of the dielectric ε_i) connected in series. For a multilayer consisting of five alternations of each a material layer d_1, ε_1 and a material layer d_2, ε_2 this results in the total capacitance $C_{\text{total}} = \frac{\varepsilon_1 \varepsilon_2 \cdot \varepsilon_0 \cdot A^2}{5(\varepsilon_1 d_2 + \varepsilon_2 d_1)} = \varepsilon_{\text{theo}} \varepsilon_0 \frac{A}{d_{\text{total}}}$ with $\varepsilon_{\text{theo}} = \frac{\varepsilon_1 \varepsilon_2 \cdot (d_1 + d_2)}{\varepsilon_1 d_2 + \varepsilon_2 d_1}$ and $d_{\text{total}} = 5 \cdot (d_1 + d_2)$ (Fig. 5.3 right). Alternatively an average permittivity ε_{avg} can be calculated, considering the relative amount of both materials (Fig. 5.3 center).

Four multilayer systems have been examined (see Tab. 4.5) and for each the theoretical effective permittivity $\varepsilon_{\text{theo}}$ and the average permittivity ε_{avg} are calculated based on the GPCs of the individual processes and assuming a relative permittivity of $\varepsilon = 8.5$ for Al_2O_3 and $\varepsilon = 34$ for TiO_2. For the first system (5 alternations) $\varepsilon_{\text{theo}} = 10.5$ and $\varepsilon_{\text{avg}} = 15.0$, while the values determined are 12.99 ± 0.75 and 13.53 ± 0.32 and thus between these two calculated values. For the second system (2 alternations) $\varepsilon_{\text{theo}} = 11.4$ and $\varepsilon_{\text{avg}} = 17.1$, while the values determined are 13.39 ± 0.65 and 13.64 ± 0.74 and thus again between the two calculated values. For the third system (3 alternations) $\varepsilon_{\text{theo}} = 11.3$ and $\varepsilon_{\text{avg}} = 17.0$ with the obtained values (13.55 ± 0.76 and 13.52 ± 0.68) again in between. For the fourth system that is the same as the first, but deposited using another machine, the obtained values of 14.33 ± 0.74 and 14.64 ± 0.50 are close to the calculated average permittivity $\varepsilon_{\text{avg}} = 15.0$. The calculated theoretical effective permittivity $\varepsilon_{\text{theo}}$ is 10.5.
This suggests the assumption that the individual layers of the multilayer are not strictly separated, but that junction regions form where the Al_2O_3 and the TiO_2 layers mix.
The multilayers withstood voltages up to 74 V before electrical breakdown occurred which is significantly larger than any voltage occurring in a flexible electrically active implant.

5.5.2 permeation measurements

In order to examine the suitability of ALD layers as barriers against gas permeation, helium based measurements on different foil samples have been performed. While the actual quantity of interest is the water vapor transmission rate through different ALD films in units of $\frac{\text{g}}{\text{m}^2\text{d}}$, within this work the helium leak rate through different ALD coated foils in units of $\frac{\text{mbar}\cdot\ell}{\text{s}}$ was measured instead. Comparison of the helium leak rate of coated and uncoated foil substrates provided the barrier improvement factor (BIF) which is the factor by which the helium leak rate decreases due to the coating. The obtained values for the BIF for different tested ALD layers on different foils were approximately in the range between 100 and 10,000. However, decrease of the BIF for repeated measurements was observed which was attributed to the formation of cracks in the ALD layers. This emphasizes the difficulties in using brittle barrier layers in a flexible device.
Measurement with helium came with the advantage of high sensitivity – allowing also the measurement of very impermeable samples – due to the low helium background. The setup allows the measurement of minimum values of approximately 10^{-10} mbar $\cdot\,\ell/\text{s}$. In addition, the small molecule size of the helium leads to fast diffusion and thus short measurement times. A typical measurement took between 5 and 20 minutes. However, after each measurement the setup had to be purged with nitrogen for at least the same time in order to regain a low background for the next measurement.
The setup allows reproducible and accurate measurements as has been shown on repeated measurements during one week. Any measurement deviations are dependent on the samples. Their preparation was also the biggest challenge in order to perform good measurements. Often damage on the foils was visible by eye and the corresponding samples were not measured. However, invisible damage of the measured samples cannot be completely precluded. Repeated measurements of the same sample led to increasing helium leak values and thus to a decline of the foils barrier properties. Increase of the measured leak rate for thin uncoated parylene C foils is attributed to the formation of micro cracks. Polyimide has a higher tensile strength and is thus more robust when mechanically stressed. Increase of the measured leak rate for ALD coated foils is attributed to a deterioration of the ALD layers' barrier properties due to their brittle nature and the strong mechanical load during measurement. For the samples based on parylene C foils thus the ALD coating was enclosed into the center of the foil at the neutral axis of the foil reducing tensile and compressive load on the brittle ALD coating. While there was still a decline of the barrier properties for these samples the decline was less than for the samples based on the $6\,\mu\text{m}$ polyimide foil, where the ALD coating was not near the neutral axis. Also the lowest absolute values measured (10^{-9} mbar $\cdot\,\ell/\text{s}$) were obtained for these samples. For the $6\,\mu\text{m}$ polyimide foils no second $6\,\mu\text{m}$ polyimide foil was added on top of the ALD coating – placing the ALD coating in the neutral axis of the sample – as this would have required baking at $350°$C. This could however have affected the crystallinity of the ALD films deposited at temperatures $\leqslant 120°$C and thus change their barrier properties.
The main problem with the measurement values, which declined with every repetition of the measurement due to mechanical stress during the measurement, is that not even the first measurement can be fully trusted, and it only provides a limiting value σ with the real value

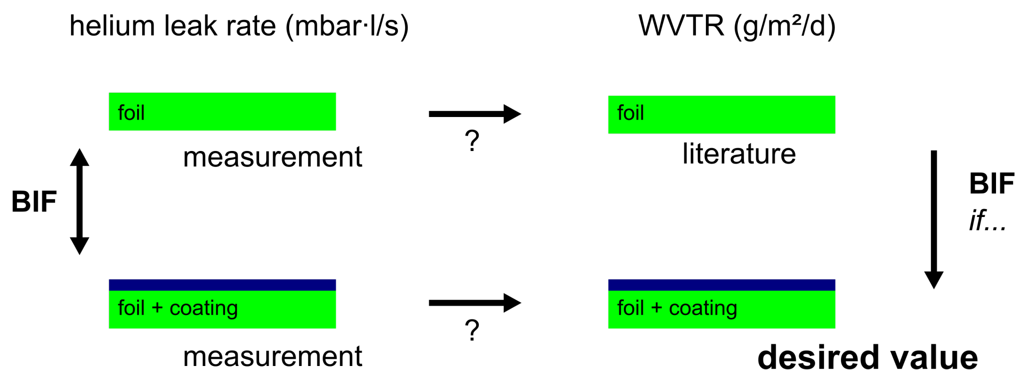


Figure 5.4: Schematic showing how the WVTR of a coated foil can be estimated from the BIF using an uncoated reference foil. The helium leak rate can be measured for an uncoated and for a coated foil. The resulting values are linked through the BIF. Direct conversion of the helium leak rate to the WVTR is not possible, but under certain conditions the WVTRs of the uncoated and coated foil are linked through the same BIF. Thus, based on a literature value for the WVTR of the uncoated foil the WVTR of the coated foil can be estimated. However, conversion is only possible if there are no diffusion paths through the coating that are exclusively available to helium or water.

$\gamma \leqslant \sigma$. Any damage due to the measurement is likely to occur when the half of the setup underneath the sample is evacuated and the sample pressed against the supporting structure with 1 bar pressure difference. Thus, the first damage has already appeared when the leak rate reaches saturation during the first measurement. Between the measurements the setup was vented and the sample newly placed and thus additional defects are caused when the measurement is started and the lower part of the setup evacuated again. It is obvious to assume that the increase of the resulting value is decreasing with any further repetition and the value might converge towards a final value for a high number of repeated measurements. This requires however that no other sources of sample damage – such as incautious handling of the sample – occur.
As the actual quantity of interest is the WVTR in units of $\frac{\text{g}}{\text{m}^2\text{d}}$ and not the helium leak rate any possibility of conversion is of interest. Under certain assumptions an easy conversion of the values providing at least the order of magnitude in units of $\frac{\text{g}}{\text{m}^2\text{d}}$ is possible. The measured helium leak rate corresponds to a flow of helium molecules through the foil for a certain difference of the helium partial pressure across the foil. The different samples thus differ in their hindrance to the helium flow. In analogy with electrical currents and Ohm's law a simple model (and easy equivalent circuits) can be developed to assess the barrier properties of a barrier coating and to estimate the effect of defects on the measurement values obtained. The quantity of interest is the resistance of the sample concerning the helium flow. The measurements provide the helium leak rate that is proportional to the helium flow through the sample and corresponds to a current. The product of helium flow and resistance of the sample depends on the helium pressure difference between both sides of the sample and is constant.

To estimate the WVTR of a coated foil a very simple equivalent circuit for the sample consisting of two resistances in series can be used. For an uncoated reference foil the resistance is R_{foil} and while the helium leak rate is obtained the WVTR can either be determined using another setup or taken from literature. For the coated foil the resistance is $R_{\text{foil}} + R_{\text{coating}} = \text{BIF} \cdot R_{\text{foil}}$

with BIF $= \frac{R_{\text{foil}}+R_{\text{coating}}}{R_{\text{foil}}}$ which for $R_{\text{foil}} \ll R_{\text{coating}}$ becomes BIF $\approx \frac{R_{\text{coating}}}{R_{\text{foil}}}$. Assuming that R_{coating} is caused by diffusion through a solid (following Fick's laws of diffusion), the helium leak rate and the WVTR should change by the same factor BIF. The WVTR of the coated foil can then be calculated as the product of WVTR of the uncoated reference foil and BIF (see Fig. 5.4). However, this way to estimate the WVTR from the obtained BIF loses validity if other diffusion processes through the ALD coating are relevant.

Permeation is a three step process starting with the adsorption of the gas molecules on the surface, followed by the diffusion through the material and ending with the desorption on the other side. As the diffusion usually is the slowest process it determines the process. Defects such as cracks or pinholes can open up additional diffusion paths besides the diffusion through the solid that can differ for different gases. Molecules of the gas can condense on the material and for example diffuse on the surface of a pinhole. Such diffusion paths are more relevant for water molecules than for helium atoms. Thus, the conversion of the helium leak rate into a WVTR following the above mentioned approach probably provides only a lower limit: $\text{WVTR}_{\text{real}} \geq \text{WVTR}_{\text{calc}}$ which is not useful. Further, even if a valid conversion factor was known in the beginning (e.g. because it can be assumed that at the beginning there are no defects and thus no additional diffusion paths) it would lose its validity when the barrier properties decay for repeated measurements. This is because the damage of the barrier leading to the decay of barrier properties is due to the formation of additional diffusion paths that are different for helium and water and thus $\text{BIF}_{\text{He}} \neq \text{BIF}_{H_2O}$. Concerning the material of the uncoated reference foil it is important to take permselectivity of polymers into account e.g. different polymers have different conversion factors for the permeation of different gases. Therefore, the reference foil has to be of the same material as the foil of the coated sample.

The method is fast and very sensitive. The samples are flexible foils of the same material as they are used in a flexible electrically active device and thus they are close to the aimed field of application for the barrier coatings. The setup allows reproducible measurements and provides comparable measurement values. Yet, conversion of the obtained helium leak rates into WVTRs is only possible within limits. Also, problems with increasing values for repeated measurements on the same sample indicate the damaging of the samples during measurement due to mechanical stress on the samples. Thus, the obtained values in these cases are probably below the theoretical performance of the sample. Still, the measurement method is suitable to examine the barrier properties of foils coated with different inorganic barrier coatings. It is however essential to keep in mind the limitations of the method, especially concerning the conversion of the values into WVTRs. And the preparation of the samples is a key process concerning the measurement and has to aim for samples that are not affected by the mechanical stress during measurement and thus provide constant values for repeated measurements. This is however also in the interest of any application of the barriers in a flexible device where the barrier abilities should also not decrease.

For all performed measurements performed on ALD coated foils a decreased helium leak rate compared to an uncoated reference foil was observed. The best results were obtained for the samples consisting of a parylene/ALD/parylene stack, so that the ALD layer was in the neutral axis of the sample. The best value obtained was $1.4 \cdot 10^{-9}$ mbar $\cdot\, \ell$/s corresponding to a BIF of 18,571. Also, this value changed only little for repeated measurements in the sense,

that is stayed within the same order of magnitude. Thus, for this value an estimation of the corresponding WVTR in units of $\frac{\mathrm{g}}{\mathrm{m^2d}}$ following the above mentioned approach shall be given. Starting from a WVTR of the reference of $\approx 12\,\frac{\mathrm{g}}{\mathrm{m^2d}}$ based on a literature value [169] the WVTR of the sample with ALD coating is $\approx 6.5 \cdot 10^{-4}\,\frac{\mathrm{g}}{\mathrm{m^2d}}$. It is easy so see that a leak rate in the range of $10^{-8}\,\mathrm{mbar} \cdot \ell/\mathrm{s}$ would accordingly result in a WVTR in the range of $10^{-3}\,\frac{\mathrm{g}}{\mathrm{m^2d}}$. But, for the cases where a leak rate of $10^{-8}\,\mathrm{mbar} \cdot \ell/\mathrm{s}$ was initially measured, but the value increased to $10^{-6}\,\mathrm{mbar} \cdot \ell/\mathrm{s}$ in the third measurement the BIF can then no longer be used to estimate the WVTR during this third measurement, because it is likely that new diffusion paths have formed that behave different for helium and water vapor.
For some samples (parylene/ALD/parylene) the helium leak rate did not reach saturation for the first measurement, while saturation was regularly reached for any further measurement. A possible explanation is the sample composition (two parylene layers, one ALD layer). For the ALD layer and the second parylene layer the final saturation value can just be reached, when the foregoing layer has reached saturation. This would also explain the observed two regimes of linear increase with different slopes. It is then however not evident why saturation is reached fast for any further measurement. Another explanation could be, that the increase is due to the formation of defects in the ALD layer and thus the formation of additional diffusion paths while under constant stress during the measurement. For any further measurement the defects have already formed and thus there is then no further increase in leak rate or the effect is then no longer significant, respectively. An explanation why this was not observed for the samples based on the $6\,\mu\mathrm{m}$ polyimide foil could be that there the ALD coating was stressed and compressed as it was not in the neutral axis and thus a large number of defects did directly form at the beginning of the measurement.
The total resistance provided by the sample can – in a simple model – be attributed to four components. The resistance of the uncoated polymer foil, the resistance of the ALD layer, the resistance of the polymer foil where it is damaged and the resistance of the ALD layer at a defect or where it is damaged. It is obvious that in an equivalent circuit of the sample the resistances of the intact layer and the damaged layer are in parallel and that the resistances of different layers (e.g. foil and ALD layer) are in series. Neglecting any diffusion component parallel to the layers (assuming thin films) the total resistance of the sample is modeled by four paths in parallel (see Fig. 5.5). Setting all constants of proportionality to one and normalizing everything to the measurement area they can be modeled by the quotient of their specific resistance (the resistance for the case that the complete cross section of the measurement area was made of this path) and their real area share. The specific resistance of the first path, which is through the intact foil and the intact ALD layer is R_0, its share is a_0. The specific resistance of the second path, which is through a damaged ALD layer on top of an intact foil is $R^\star_{\mathrm{ALD}}$ with share $a^\star_{\mathrm{ALD}}$. The third path, which is through an intact ALD layer on top of an damaged foil, has the specific resistance $R^\star_{\mathrm{foil}}$ and share $a^\star_{\mathrm{foil}}$ and the fourth path, which is through a damaged ALD layer on top of an damaged foil, has the specific resistance $R^\star$ with share $a^\star$. Therefore, the total resistance of the sample is $R_{\mathrm{sample}} = \frac{1}{a_0/R_0 + a^\star_{\mathrm{ALD}}/R^\star_{\mathrm{ALD}} + a^\star_{\mathrm{foil}}/R^\star_{\mathrm{foil}} + a^\star/R^\star}$.
While the specific resistances have firm values, the shares of the different paths can change when the sample is mechanically stressed. As the resistance introduced by the ALD coating is assumed to be greater by several orders of magnitude than the resistance of the foil, the specific

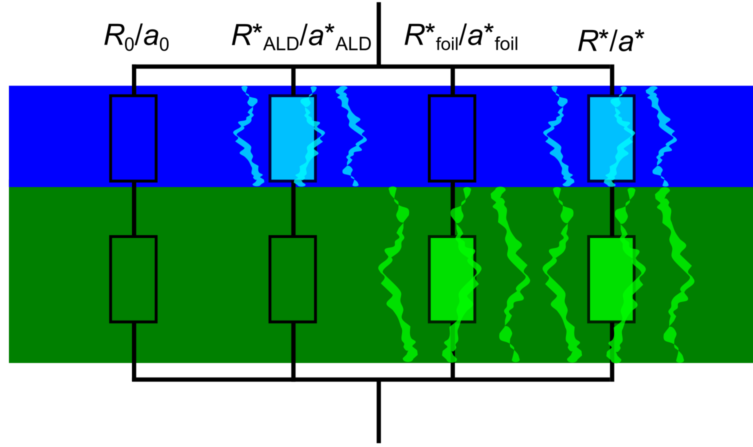


Figure 5.5: Schematic showing a simple equivalent circuit for the diffusion through an ALD coated foil. A higher resistance corresponds to slower diffusion and thus a better barrier. The first path represents the ideal case with coating and foil being defect free, the specific resistance of this path is R_0, its share is a_0. The second and third path represent the case for either coating or foil containing defects. The fourth paths represents the case for coating and foil containing defects e.g. cracks.

resistances of the intact sample and the intact ALD coating on a damaged foil are almost equal $R_0 \approx R^\star_{\text{foil}}$. As value – all units set to one – the reciprocal of the minimal measured leak rate is taken, and thus $R_0 = R^\star_{\text{foil}} = 10^9$ is assumed. $R^\star_{\text{ALD}}$ corresponds to an almost uncoated foil and thus the the reciprocal of the leak rate of an uncoated foil $R^\star_{\text{ALD}} = 10^5$ is taken as its value. The value for the case of a damaged coating on a damaged foil can be estimated from the maximum values measured for damaged samples and thus $R^\star = 10^3$ is assumed. The shares of the four paths are estimated relating to the measurement area of $380\,\text{mm}^2$. The share of the intact area with both foil and coating undamaged is $a_0 = 1 - a^\star_{\text{ALD}} - a^\star_{\text{foil}} - a^\star$. For $a^\star_{\text{foil}}$ a total defect area of $(100\,\mu\text{m})^2$ is assumed, resulting in $a^\star_{\text{foil}} = 10^{-5}$. The area where foil and ALD coating are damaged is assumed to be even less $(100\,\text{nm})^2$ and thus $a^\star = 10^{-11}$. At the beginning (prior to the first measurement) the area where the ALD coating is damaged is assumed to be very small and thus $a^\star_{\text{ALD}} = 10^{-11}$ is assumed.
These values then result in a total resistance of the sample of $R_{\text{sample}} = 1.00 \cdot 10^9$ and thus a leak rate of $1.00 \cdot 10^{-9}\,\text{mbar} \cdot \ell/\text{s}$ would be measured. However, the mechanical load during the measurement can damage the brittle ALD coating and thus change the share $a^\star_{\text{ALD}}$. The area where the layer gets damaged can be estimated from a ring with the circumference of the support structure and a width of $100\,\mu\text{m}$, which corresponds to a gap at the end of the support structure causing bending and thus damaging of the sample. This then results in an increased share $a^\star_{\text{ALD}} = 10^{-2}$. The total resistance of the sample would then be $R_{\text{sample}} = 9.90 \cdot 10^6$ and thus a leak rate of $1.01 \cdot 10^{-7}\,\text{mbar} \cdot \ell/\text{s}$ would be measured. For any further measurement the same area would be additionally damaged and thus for the next measurement the share would be twice as big $a^\star_{\text{ALD}} = 2 \cdot 10^{-2}$ which would result in $R_{\text{sample}} = 4.98 \cdot 10^6$ and thus a measured leak rate of $2.01 \cdot 10^{-7}\,\text{mbar} \cdot \ell/\text{s}$.
This shows, that damage of the coating produced by the measurement has a very big impact on the measured initial value, but becomes less significant for any further measurement. Thus, it

is valid to assume that the measured leak rate would converge towards a fixed boundary value when the measurement is repeated many times. The model fits very well with the observed behavior of the samples for repeated measurements.
So, while the obtained results prove good barrier properties of the ALD coatings more successful measurements need to be performed to allow statements on the differences between different ALD coatings (concerning thickness, material, and multilayer composition). An idea to overcome the problems during sample preparation would be to detach the parylene foils prior to the ALD deposition. Gluing them to a substrate with tape can prevent layer deposition on the backside of the sample during ALD deposition and the deposition of the second parylene layer, while the sample can easily be removed from the handle substrate at the end.

5.6 fabrication of the Neuroflexarray

All processes discussed above in sections 5.1, 5.2 and 5.3 aimed for the fabrication of the Neuroflexarray as a new type of MEA based on an array of embedded dies each only $\approx 250\,\mu\mathrm{m} \times 250\,\mu\mathrm{m} \times 200\,\mu\mathrm{m}$ in size. To develop the fabrication processes and prove feasibility, a demonstrator system based on die-dummies was drafted (sec. 3.1.1) and fabricated. All fabrication steps could be conducted on the samples and thus the system could be completely built. Regarding the complex fabrication process with so many steps this cannot be taken for granted and is thus a great success. However, at the end starting delamination could be observed, showing also that at the end of the fabrication process also the limits of the samples endurance was reached. Thus, the fabrication of more complex system containing e.g. three layers of conducting tracks seems not only unreasonable due to the elaborate process but also problematic concerning the stability of the samples. Also it is obvious that the adhesion between the different material layers must be increased to obtain a device that is not only stable enough to survive the different fabrication steps, but also stable under the harsh and humid environmental conditions given by an application of the device.
While all fabrication steps could be conducted to finish the system, the results of the individual fabrication steps were not always satisfying. While the layout of the demonstrator system included test structures to allow proof that the die-dummies are electrically connected and to determine the electrical resistance of the conducting tracks and the VIAs, no such measurements could be performed on the finished samples. The obtained resistance was always above the measurement limit and thus $> 20\,\mathrm{M\Omega}$. Each test structure spanned on both layers of conducting tracks and thus always included VIAs between these two layers. While short circuits due to incompletely structured tracks and interruptions of tracks (e.g. at cracks in the surface) can easily be seen, bad electrical contact at the VIAs is less visible. Even a few 100 nm of remaining parylene C can cause a high-resistance contact at a VIA. During the etching of the VIAs it is however difficult to see, if the parylene is completely etched, because it is colorless and can thus only be seen if interference occurs for very thin parylene layers. Further the VIAs are so small in diameter that a thorough examination is not possible. It might also be that the conducting tracks could not completely follow the steep flank angles of the VIAs and thus there is very bad or even no electrical connection. So, altogether the fabrication of the demonstrator was not successful

concerning a functional device. Yet, also during the fabrication individual steps could be further optimized and thus based on the experience of this single complete run a better result seems likely in any further trial. The laborious fabrication process with its high number of individual fabrication steps makes the overall fabrication process prone to errors. Also, the result of the embedding process has a very strong influence on all following lithographic fabrication steps and thus further improvement of their result can to some extent only be achieved by optimizing the embedding process. This makes it also difficult to quickly implement improvements.
A central point for the transfer printing process was the achieved yield of transferred dies. Due to misplacement of individual dies of the array, the effective yield could be lower than the number of transferred dies divided by the total number of dies of the complete array. While this topic has been discussed above, it is of interest here if the number of dies included into the total system was further decreased during the following fabrication steps. Concerning the alignment within the different fabrication steps based on photolithography, there was no further "loss" of dies after the alignment of the first photomask (first VIA layer). All further photomasks could be aligned on the structures of previous photolithographic fabrication steps. Thus, alignment on the dies was proper for all dies if the alignment was proper in the first case, but bad alignment did not occur for any further die of the array. This means that the "effective yield" was not further lowered during the alignment steps. The fabrication processes for the VIAs and the conducting tracks were parallel to all dies of the array and thus they in general were successful for all dies or none of the dies. However, it was possible that due to inhomogeneities in the layer thickness of the hardmask or the parylene the required etching times varied between different locations on the sample. A control between the different fabrication steps should however prevent the functional loss of dies due to this effect.
All fabrication processes based on photolithography have been chosen to be based on bright-field masks. While this is a usual choice for the fabrication of the conducting tracks that are dry etched against a positive tone photoresist mask, it is an uncommon choice for the fabrication of the VIAs. For the first VIA layer the bright-field mask was chosen to allow easy alignment of the mask on the array with no alignment markers available. Thus, the choice there is beyond doubt. For the other two VIA layers this uncommon choice was only made to avoid an additional process with another resist. Yet, other processes – based on a dark-field mask – are a legitimate choice there too. Due to the observed formation of cracks when etching the parylene against a thick resist mask, the structuring of a hardmask seems inevitable. The use of a dark-field process would require the use of a positive tone resist. This would also be the usual choice for such a process, as in a negative tone resist process any particle on the mask shading the resist leads to an unwanted hole etched into the parylene. However, for the processes having access to alignment markers full sight of the relevant area with the possibility to align the mask on the structures was useful and thus an additional process for the etching of the second and third layer of VIAs based on a dark-field mask appears as not beneficial.
As the negative tone resist used for the structuring of the VIAs never showed problems concerning the surface topography of the samples, the fabrication of the conducting tracks based on a negative tone resist and the same bright-field mask, using a lift-off process, appears as a smart alternative for the fabrication of the conducting tracks. Yet, lift-off with metal films deposited by sputter deposition is challenging and requires sophisticated processing. The edges

of the resulting tracks can protrude from the surface. So, while this path appears promising on first sight, reconsideration reveals that it needs probably the same amount of development and optimization as the chosen process based on dry etching.
The system has been completely fabricated on top of a rigid glass handle substrate. In order to obtain a flexible device the system has to be detached. During the development of the fabrication process this has been treated as a task that can be handled separately. It requires at least two steps. The three top parylene layers cover also the edges and the backside of the glass handle substrate and thus the complete system needs to be cut out on the desired contour. Then, the stack needs to be detached from the handle substrate it is attached to with the PDMS. This might require a release layer. As this release layer has to be present during the complete fabrication process after the embedding process is faces several constrains. First of all it has to be durable. Shellac and resist cannot be used as a release layer, because of the embedding process. At the end of the embedding process the old handle substrate is detached using a shellac layer as release layer, while the system has to stick to the new handle substrate that should therefore only have a release layer not affected by this process. Possible release layers are metal films (e.g. aluminum) that can be etched away fast. Anodic metal dissolution based on electrochemical metal removal in a nontoxic salt solution is a possibility to quickly remove a metal film (e.g. aluminum) by applying a current [184]. Such a process seems also suitable for the release of the Neuroflexarray.
The main motivation of the project "NEURO-FLEXARRAY" was the development of a microelectrode array allowing higher electrode numbers as passive MEAs for the same electrode density. Multiplexing of the signals in the embedded dies shall therefore reduce the number of required conducting tracks limiting the size of passive MEAs. While only a demonstrator system with functionless die-dummies was built, it was designed to imitate the system with functioning dies. These dies will only multiplex the signals of the 25 electrodes of one cluster, and thus the array will not be arbitrarily scalable. This would require multiplexing between all electrodes of the array and thus the different clusters. However, at some point there will then also be limitations concerning the temporal resolution. Still, the Neuroflexarray in this form already considerably enhances the maximum number of electrodes of an array. The electrode density of an array is $\rho = 1/d^2$ with the electrode pitch d. The maximum number of electrodes in one array N depends on ρ. The limiting factor – in a passive MEA – is that all tracks connecting the electrodes of one row of the array at the first column of the array have to pass between the electrodes of this row and its neighboring row. As each track requires a space s consisting of its width and the spacing to the neighboring track, there can be d/s tracks and thus for a quadratic array with the tracks leaving the array only on one side a passive MEA can have $N = (d/2)^2 = k/\rho$ electrodes with $k = 1/s^2$. The constant of proportionality k thereby expresses the relationship between the maximum number of electrodes and the electrode density. When the tracks are allowed to leave the array on all four sides this array can of course be mirrored, allowing a quadratic array of approximately four times the size. Also, in this layout only the number of columns, not the number of rows is limited. For the Neuroflexarray in this form the maximum electrode number for a given electrode density is higher. It is 25 times the maximum number of clusters the array can contain, as the size is limited by the number of dies that each support 25 electrodes. Each cluster of the array will include one

track that has to be guided separately limiting the size of the array. In addition there are tracks that do not limit the size of the array, as their number does not increase with the number of tracks. However, these tracks require d space. The layout allowed the guiding of all tracks in a form leaving then $3 \cdot d$ of space for the guiding of the tracks limiting the size of the array. Thus, $N = 25 \cdot (3 \cdot d/s)^2 = k \cdot 1/\rho$ with $k = 225/s^2$. So in comparison to the passive MEA the Neuroflexarray will – for the same electrode density – allow a 225 times higher electrode number.

Chapter 6

Conclusion and Outlook

In this last chapter conclusions concerning the potential of the developed fabrication process are drawn. It is evaluated what the developed process can afford and what the observed properties of the ALD layers mean, with respect to their possible use to increase the longtime stability of a flexible electrically active implant. In addition an outlook is given on where within the developed process is the highest potential for improvement and what has to be changed for a reliable commercial usable fabrication process. At the end, the opportunities of the developed process and the devices that can be fabricated using this process are highlighted.

6.1 conclusion

A fabrication process for a flexible chip-in-foil system has been developed including all steps from the transfer and the embedding of dies as well as the structuring of conducting tracks and VIAs on top. The process was applied to the fabrication of a demonstrator system consisting of an array of 49 die-dummies, representing a MEA with 1225 electrodes. While all process steps could be conducted, several steps especially those concerning the structuring of the conducting tracks require further improvement. The electrical connections in the finished demonstrator system were not fabricated properly but included interruptions and short circuits. Yet, these problems occurred due to the long lasting and complex process and should easily be overcome with further optimization of a few fabrication steps.
The technology is also applicable to other similar devices. For the Neuroflexarray an array of thick dies that were very small in area have been embedded, but the process is also applicable to thin dies that are larger in area. The thickness of the fabricated system is primarily determined by the thickness of the dies.
Structuring of the electrical connections on top of the embedded dies was not possible using simple standard processes, but required the development of more elaborate processes. One failed process step can cause failure of the resulting device.
Longtime stability is a key concern for flexible electrically active implants. For the fabricated device this requires improvement of the adhesion between the different material layers, especially the adhesion of parylene C on parylene C is of central importance. Within this work the feasibility of ALD coatings as water vapor barriers was shown. However, their integration

into the fabrication process is still needed. Due to their brittle nature their position in the fabricated device is critical. The position of the neutral axis of the system – facing no tension or compression during bending – can be engineered by varying the thickness of the PDMS and the parylene layers. An unsolved problem concerning the stability of the fabricated device are its open edges if it is cut out, to detach it from the rigid handle substrate it is fabricated on. They provide paths for easy water diffusion inside the device.

6.2 outlook

So far only a demonstrator system with inoperable die-dummies was built. However, the layout of the demonstrator system was drafted in a way that the direct applicability of its fabrication process to the real Neuroflexarray with the functioning dies is guaranteed. Thus, successful fabrication of the demonstrator system will immediately allow the fabrication of the Neuroflexarray.
Still, some conclusions can be drawn, where there is potential for improvement concerning the fabrication process as well as the fabricated device.

6.2.1 potential for improvement

While for a research project a proof of principle is sufficient, commercial exploitation requires a stable process that can reliably provide complete arrays. This means arrays with also only 5% to 10% of the dies missing due to loss during transfer or misplacement are not acceptable. Also, within this work only 7×7 arrays were handled, which was an arbitrary limitation.
There are several possibilities, how the process can be improved without changing the fundamental idea of the fabrication process, by using state of the art technology that was not accessible during this work.
As every process step affects all following fabrication steps, the highest potential for improvement is right at the beginning of the process starting with the separation of the dies. Within this work wafer pieces of only $\approx 1\,\mathrm{cm}^2$ were separated into the $(250\,\mu\mathrm{m})^2$ sized die-dummies. For the separation of bigger wafer pieces or a complete wafer into such tiny dies dicing becomes problematic. Due to the small size of the dies separation requires a large number of cuts, and thus the blade ages fast. However, with increasing working life of the blade the quality of the cuts decreases. For the separation of a complete wafer this can lead to a visible increase of the kerf width on the wafer. Further, the dicing requires much time and therefore a parallel separation process – that would be too elaborate and slow for normal sized dies – becomes more attractive. Also dicing requires a relatively wide free space between the dies for dicing (kerf width). Even if only $50\,\mu\mathrm{m}$ are left free for separation, still only $\approx 70\%$ of the wafer area is used. Furthermore, another process for separation could make the turning step, between transfer printing and embedding, redundant if its final step is performed with the dies sitting upside down to an adequate donor substrate. The alignment during transfer printing can also be performed with the dies sitting upside down. And finally a separation process requiring no rinsing with water at its final stage would circumvent the risk of introduced misplacement of

dies during drying.
Possible candidates for an improved separation process are:

- stealth dicing [185], providing small kerf width but probably being incompatible with the transfer printing process due to tape expansion
- plasma dicing [186], providing excellent usage of the wafer area and being a dry process without water rinsing
- dice before grind, providing the dies upside down

Non of these processes can improve all of the aforementioned points, but each of the processes entails the potential of improvement and even more separation methods are available [187]. Some of the processes directly come with the possibility to further thin down the dies. Thinner dies would decrease the total thickness of the final system and probably would also reduce capillary forces during drying, when water rinsing is part of the process.
To improve the transfer printing process the construction of a special machine allowing control of the separation speed and assuring perpendicular contact would be advisable.
Within the developed process shellac plays a key role and has proven its high utility, also as sacrificial layer. However, it is also linked to the imperfect result of the embedding process with its remaining surface topography. If the separation process ends with the dies sitting already upside down, the turning step is not required and thus either the sugar- or the shellac-coating is no longer required. In this case the shellac-coating seems more suitable and thus should be used further. This requires adaption of the second part of the transfer printing, when the dies are transferred from the stamp to the receiver substrate. However, a new material or material combination could allow better results. If a process allowing the adhesion of the array to a surface without the formation of menisci building a form-fitting connection, a perfect flat surface would be possible. This task must not be fulfilled by the same material used as sacrificial layer at the end of the embedding process.
The combination of the developed transfer printing process with a self-alignment process [188] could increase placement accuracy of the dies. Further, as the placement accuracy would be guaranteed by the self-alignment process, it would enable to belatedly add dies that were not transferred in the transfer printing process and thus complete arrays, without any missing die, could steadily be provided.
In addition to this optimization potential concerning the fabrication process there is potential to increase the longtime stability of the fabricated device. Enhanced adhesion between the different material layers can be achieved through a sophisticated combination of plasma pretreatment and the application of silane adhesion promoters. The adhesion between different parylene C layers could possibly also be further increased by the addition of metal-oxide layers [177].
Replacement of the parylene would also reduce the adhesion problem. Building the complete device from PDMS would reduce the number of materials, and between different layers of PDMS no adhesion failure occurs. However, the insulating properties of PDMS are not as good as those of parylene. Within this work this path was not followed, because there was no clean room facility to micro machine PDMS.

The feasibility of ALD deposited metal-oxide layers as barriers against the intrusion of water vapor was shown, but their deposition has not been introduced to the overall fabrication process. This remains a task for future work.

6.2.2 opportunities of the developed process

The Neuroflexarray could be used for ECoG (electrocorticography) measurements, or as flexible electrode array with high electrode number on other soft organs in the body. The embedded dies can either allow higher electrode numbers or a reduced number of tracks leaving the system and thus can diminish the problem concerning a plug, where the tracks/cable have to leave the body. The number of electrodes can be further increased and multiplexing between the individual clusters (not only within the clusters) would change the scaling laws dramatically allowing still higher electrode numbers.
For special applications one could also design arrays with a heterogeneous electrode distribution. The clusters formed by the individual dies can be considered as building blocks, providing each 25 electrodes that can be freely distributed with the only limitation being the minimum spacing of $40\ \mu\mathrm{m}$ (spacing of the contact pads on the die).
The technology developed to fabricate the Neuroflexarray can also be used to fabricate other flexible multi-chip systems. The only precondition to the full applicability of the process is that the dies for the device must be fabricated in their correct relative positions on one wafer. While applications apart from medicine are not restricted to biocompatibility, satisfying the strong constraints for a medical implant is also useful for other fields of application dealing with harsh and humid environments.

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